# Studies on ohmic contacts to GaAs-based MESFETs and pseudomorphic HEMTs



Thesis submitted for the degree of

**Doctor of Philosophy**

*by*

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# Dedication

I wandered in solitude, endless and weary,
In strange wilderness and vague sweetness,
O'er the hills with burdened emptiness,
In search of the brink of eternity.

In moments of stillness, tremulous and desolate,
Thy voice deep within, thine enchanted presence,
Hast shown my path to the golden abode,
Hast held my being in perpetual contentment.

Blossoms I offer at thy lotus feet
In gratitude and everlasting prayer,
Prayers I offer at thy divine feet
With love and dedication.

— G. Sai Saravanan

*A humble offering*
*at the feet*
*of*
Bhagawan Sri Sathya Sai Baba

# DECLARATION

I hereby declare that the work embodied in this thesis entitled "**Studies on ohmic contacts to GaAs-based MESFETs and pseudomorphic HEMTs**" carried out by me, under the supervision of **Dr. K. Muraleedharan**, Scientist F, Defence Metallurgical Research Laboratory, Hyderabad, India, and **Prof. Anand P. Pathak**, School of Physics, University of Hyderabad, Hyderabad, India, has not been submitted for any other degree or diploma either in part or in full to this or to any other University or Institution.

**(G. Sai Saravanan)**

Place: Hyderabad

Date : 13.07.07

# CERTIFICATE

This is to certify that the work described in this thesis entitled "**Studies on ohmic contacts to GaAs-based MESFETs and pseudomorphic HEMTs**" has been carried out by Mr. G. Sai Saravanan under our direct supervision for the full period prescribed under Ph.D. ordinances of the University, and the same has not been submitted for any other degree or diploma to this or any other University or Institution.

13.7.02

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# Chapter I

# Introduction

*This chapter presents an outline of the theory and literature pertaining to ohmic contacts to GaAs-based MESFETs and pseudomorphic HEMTs, and influence of activation annealing on ohmic contacts The motivation and objectives of this thesis are listed The chapter concludes with the thesis plan*

## 1.1. GaAs-based devices and MMICs

**ME**tal Semiconductor **F**ield **E**ffect **T**ransistors (MESFETs) and **P**seudomorphic **H**igh **E**lectron **M**obility **T**ransistors (pHEMTs) are fabricated using n-type GaAs device layers and operate in the microwave frequencies. These are used as active devices in **M**onolithic **M**icrowave **I**ntegrated **C**ircuits (MMICs).

### 1.1.1. MESFETs

In MESFETs (figure 1.1), the current through two terminals is controlled by a voltage at the third terminal. This control voltage, known as *gate voltage*, varies the depletion width of a reverse-biased Schottky or rectifying metal-semiconductor junction.

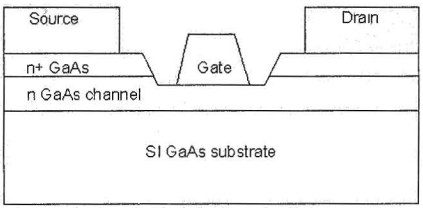


**Figure 1.1. Schematic of a MESFET showing the active layers and the contacts.**

The terminals through which current flows are the *source and drain ohmic contacts.* When a reverse bias $V_g$ is applied to the gate, the depletion region penetrates into the channel and reduces current. The depth of depletion extending into the semiconductor is a function of the doping profile and applied voltage. This depletion region acts as an insulator between the gate metal and the undepleted semiconductor region. The depth of depletion region, ω, is given by

$$\omega^2 = \frac{2\varepsilon}{qN}(V_{bi} - V_g) \qquad (1.1)$$

where $\varepsilon = k\varepsilon_0$ is the permittivity of the medium, k is the dielectric constant, $\varepsilon_0$ is the permittivity of free space, q is the magnitude of electronic charge, N is the doping concentration, and $V_{bi}$ is the built-in potential. The gate voltage at which the channel is completely depleted of carriers is known as the *pinch-off voltage*, $V_p$. This voltage naturally depends on the channel width. The *maximum or peak current*, denoted as $I_m$, is the current that will flow when gate is forward biased. The bias applied to gate, thus, controls the maximum flow of source-drain current through the channel. The fact that a large change in current occurs for a small change in gate voltage allows the MESFET to be used as an amplifier. This type of FET operation is known as the depletion mode FET [1].

The commonly used MESFET structures are made by ion implantation. The semi-insulating substrate is implanted with silicon of different doses and energies. The n-GaAs channel is formed with a carrier concentration of about $10^{17}cm^{-3}$ and the top surface layer is doped to $10^{18}cm^{-3}$.

### 1.1.2. Pseudomorphic HEMTs

In conventional MESFETs, electrons share the same space with the positively charged donor impurities and interact with the impurities. To obtain high speed and high current conditions, doping levels are to be increased, which increases ionized impurity scattering. Hence, mobility of electrons is impeded and limits the use of the transistor to frequencies upto 18GHz. This was overcome in a HEMT device by 'modulation doping' where the channel obtains the electrons from a doped, adjacent AlGaAs layer, and are confined in a 'two-dimensional electron gas' or 2DEG layer formed at the heterointerface [2]. HEMT with a channel of InGaAs quantum well between the AlGaAs Schottky layer and GaAs buffer layer is called as a *'pseudomorphic' HEMT* (figure 1.2).

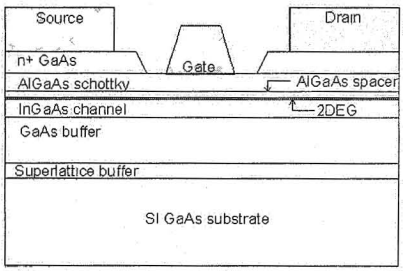


**Figure 1.2. Schematic of a pHEMT. Different layers and contacts are shown.**

When a gate bias is applied, very high mobilities and large electron velocities are obtained for small values of drain voltages. A high electron density ($\sim 10^{12}cm^{-2}$) in

a very thin layer (<100Å thick) is present close to the gate electrode, without the effects of impurity scattering. Undoped $In_xGa_{1-x}As$ layer of thickness 50 - 200Å is grown with lower indium mole fraction, (x = 0.15 – 0.35) to minimize lattice mismatch. PHEMTs demonstrated superior power gain and low-noise RF performances due to the properties of the InGaAs layer [3].

A '*planar doped*' or '*δ-doped*' Si layer with very high doping levels of about 4 - 6 x $10^{12}$ $cm^{-2}$ is grown to avoid doping of the AlGaAs Schottky layer which results in poor device breakdown voltages. As a result, the AlGaAs layer can be doped to very low levels or even grown intrinsic. HEMT structures are generally grown by molecular beam epitaxy (MBE).

### 1.1.3. Monolithic microwave integrated circuits

MMICs combine functions such as amplification, switching, filtering, etc., using various active and passive circuit functions [4]. The circuits using active and passive components are fabricated monolithically on the same semi-insulating GaAs substrate. Capacitor, resistor, inductor and transmission line are the passive devices. The conducting active layers on the wafer are either ion implanted or epitaxially grown. The typical fabrication process involves various lithography, etching, metallisation steps, and heat cycles [5].

During each stage of fabrication, different parts of devices and circuits take shape. Resistors are formed by defining GaAs active areas or by using thin resistive metal films such as nichrome. Three different levels of metallisations are used on the front side of the wafer, viz., ohmic (for source-drain contacts), Schottky (for gate electrodes), and interconnect (for connecting devices within the circuit). Capacitors are formed by using the gate metal as the bottom plate, and the interconnect metallisation as the top plate. The dielectric used for the capacitor is also used to isolate the different metallisations and crossovers. Inductors are formed by deposition of metallisation in a spiral form. Interconnects are also known as transmission lines as they conduct the microwave signals. After completion of front side fabrication, the wafer is thinned from its backside and metallised. This metallisation serves as the ground plane for microstrip components in the MMIC. Thicker backside metallisation by electroplating is also used as heat sink for power MMICs.

High uniformity of electrical performance within a wafer and wafer-to-wafer, elimination of internal wire bonding excepting the connections needed to link the IC to the outside world, and the capability of large volume production at lower costs are the attractive features of MMICs.

### 1.1.4. Applications of MMICs

The most common applications are as amplifiers, switches, phase shifters and attenuators. As amplifiers, they are used as low noise, small signal, medium power and high power amplifiers. The switches such as single pole single throw (SPST), single pole double throw (SPDT), etc., and phase shifters and attenuators are made using deeper channels in the MESFETs.

MMICs have major military and space applications, and limited applications in commercial microwave systems. The significant military applications are in signal intelligence, radar, phased arrays, electronic warfare (EW), image processing, wideband communication, low-noise amplifiers, missile seekers, ground-based communications, satellite communications, etc. Active element phased-array radars employ antennas with thousands of individual transmit-receive (T/R) modules for electronic steering. T/R modules are mostly made up of MMICs, typically consisting of low noise amplifiers, different types of power amplifiers, phase shifters, attenuators, switches, and other passive components. EW systems require wideband MMIC components, since a present-day radar-warning receiver typically covers the entire frequency band from 1GHz to 18GHz. Satellite communication receivers specially use very low noise amplifiers and power amplifiers. Satellite-mounted radars typically use hundreds of T/R module elements.

While pHEMTs can deliver very high power levels, they are also preferred for low noise applications. The useful frequency of operation of pHEMTs extends upto 40GHz.

These components undergo stringent reliability tests as they are generally used for military and space applications.

### 1.2. Ohmic contacts to n-GaAs

In principle, two types of metal-semiconductor contacts are possible. Contacts with linear characteristics are called *ohmic contacts* while those with rectifying current-voltage characteristics are called as *Schottky contacts*. The metal-semiconductor junctions in ohmic contacts conduct equally in both directions. They aid current flow in the device through the source and drain electrodes, without interfering the characteristics of the device. Ohmic contacts have very small contact resistances compared to the bulk resistance of the semiconductor.

Any metal in contact with GaAs forms rectifying contacts and heat treatment is necessary to obtain ohmic contacts. This is a complex process involving choice and thickness of metallisation, annealing conditions and nature of diffusion of constituents of metallisation. In MMICs, ohmic contacts are formed on the source and drain of MESFETs, and also on the electrodes of the resistors. This is one of the most critical components of MMICs as the device performance is influenced by the nature of contact formation.

#### 1.2.1. Ohmic contact theory

The I-V characteristics of a metal-semiconductor contact are governed by the transport of the charge carriers across the interface and its associated space-charge

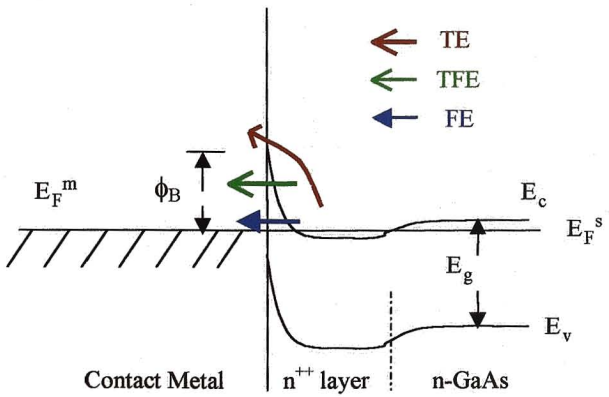


**Figure 1.3. Schematic representation of energy-band diagram of an alloyed ohmic contact with high doping. Current flow mechanisms of thermionic, thermionic-field and field emissions are indicated.**

region. Depending upon the semiconductor, its doping, temperature and $\phi_B$, current flows by mechanisms such as thermionic emission, field emission or a combination of both, known as thermionic-field emission (figure 1.3) [6]. $\phi_B$ is the energy necessary for electrons in the metal to acquire so as to penetrate the semiconductor [7].

In thermionic emission, for an n-type moderately doped GaAs under forward bias, assuming $q\phi_B >> kT$, the electrons emitted over the barrier will be in equilibrium with the electron population in the semiconductor. If V is the forward voltage applied across the Schottky diode (formed between the metal and GaAs), the current density, J, across the barrier is given by

$$J = A^{**}T^2 \exp\left(\frac{-q\phi_B}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right)-1\right]$$

$$= J_s\left[\exp\left(\frac{qV}{kT}\right)-1\right] \qquad (1.2)$$

$$J = J_s \exp\left(\frac{qV}{kT}\right), \text{ for } V >> kT/q$$

$$J = J_s \exp\left(\frac{qV}{nkT}\right) \qquad (1.3)$$

where, $A^{**}$ is the effective Richardson constant, q is electron charge, T is the absolute temperature, k is Boltzmann constant, and, n is the ideality factor, representing departures from an ideal Schottky junction (n = 1). The value of n increases with higher doping and the barrier tends to be a more leaky Schottky barrier. Contacts operating by thermionic emission are not efficient ohmic contacts.

The second and important case describes a contact on GaAs with very high doping levels where appreciable field emission is possible. As the width of the depletion layer decreases with increasing doping, quantum-mechanical tunneling can occur through the barrier. The transmission probability P that an electron of energy E can successfully tunnel through a triangular-shaped potential energy barrier with diffusion potential $V_d$ is given by

$$P = \exp\left(\frac{-2(qV_d - E)^{1/2}}{3E_{00}(qV_d)^{1/2}}\right) \qquad (1.4)$$

where, the current density is given by

$$J \approx \exp\left(\frac{-q\phi_B}{E_{00}}\right) \qquad (1.5)$$

and

$$E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N_D}{\varepsilon m^*}} \tag{1.6}$$

ħ is the Planck's constant divided by $2\pi$, ε is the dielectric constant, $N_D$ is the doping concentration, and $m^*$ is the effective electron mass. The parameter $E_{00}$ has the dimensions of energy. The tunneling current increases as the square root of doping. This is due to decrease in barrier width with the square root of doping concentration.

Thermionic-field emission is an intermediate case. Here, tunneling occurs when the electrons possess enough energy to reach the narrower part of the barrier at the top.

At very high doping or at low temperatures, where $E_{00} >> kT$, electrons are field-emitted directly from states at the Fermi level $E_F^s$ in semiconductor to vacant states in the metal. At moderate doping levels and temperatures, where $E_{00} \sim kT$, electrons tunnel at energy $E_m$ relative to the lower edge of the conduction band in the bulk. When doping is low, the carriers are thermionically emitted over the barrier with kinetic energies greater than $V_d$, where $E_{00} << kT$. The crossover from thermionic emission to thermionic-field emission occurs at low doping concentrations of the order $10^{17} - 10^{18}$ $cm^{-3}$ [8]. This is primarily due to lower value of electron effective mass in GaAs.

Tunneling enables very low resistance contacts. As *ohmic contacts* are defined as metal-semiconductor contacts exhibiting a linear J-V characteristic over a useful range of J, the non-linear J-V characteristic is of the form

$$J = J_s\left[\exp\left(\frac{V}{V_0}\right) - 1\right] \tag{1.7}$$

where, $V_0$ and $J_s$ depend on the mechanism of current flow. At very low voltages, (i.e., $V << V_0$)

$$J \approx J_s\left(\frac{V}{V_0}\right) \tag{1.8}$$

the contacts can assume a linear J-V behaviour, ignoring the dependence of $J_s$ on V. Practically, $J_s$ must be large so that the resistance of the contact is small, maintaining $V << V_0$ under all operating conditions. The largest value of $J_s$ occurs for field emission where the doping is very high. Hence, very low contact resistances are

achieved on contacts made on highly doped GaAs layers so that tunneling is significant [9].

Specific contact resistance, $r_c$, is defined as

$$r_c \equiv \left(\frac{\partial V}{\partial J}\right)_{V=0} \tag{1.9}$$

with units of $\Omega$-cm$^2$. As many device applications require very low contact resistances, $r_c \leq 10^{-6}$ $\Omega$-cm$^2$, $N_D$ must be greater than 6 x $10^{19}$ cm$^{-3}$ for n-GaAs [7].

In the above situations, current flow through the barrier is caused by a potential difference across the barrier and, decrease of this potential difference is the major practical task in ohmic contact formation. To achieve very low contact resistances, either a small $\phi_B$ or a large $N_D$ is required. The viable option is to obtain large $N_D$, and is usually implemented by using a thin $n^+$-GaAs region between the contact metal and the active (channel) layer. The channel of a MESFET is normally doped to have a concentration of about $N_D = 2 - 3 \times 10^{17}$cm$^{-3}$, which by itself would not lead to a thin barrier to facilitate tunneling. Thus, an $n^+$ layer with concentration $N_D \geq 2 \times 10^{18}$cm$^{-3}$ is formed over the active layer on which the ohmic metal would be placed [10]. In such a case, the metal-semiconductor barrier would present a small resistance and current flows freely from metal to semiconductor and vice versa.

### 1.2.2. Practical ohmic contacts

The tunneling model does not sufficiently explain the low values of contact resistivity being achieved for n-GaAs devices. It was shown that the typical values of $r_c$ for n-GaAs are much lower for a given $N_D$ than predicted by the tunneling model [10]. This is probably due to the fact that alloying process modifies the metal-semiconductor junction, and therefore, is not planar.

In principle, most of the methods of contact formation consist of deposition of a stack of thin metal layers consisting of an alloy, on highly doped surfaces and a subsequent heat treatment above the melting point of the constituent alloy. The resultant degenerate surface layer reduces the effect of barrier at the interface. The metallisation consists of AuGe (12% Ge by wt.) in an alloy form, melting at about 363°C, deposited by evaporation as the first layer. Depositions of a nickel layer and an over-layer of gold follow this. This top gold layer serves as a non-reactive, inert layer, which can be easily combined with interconnect metallisation. Alloyed ohmic

contacts using AuGe/Ni were originally introduced and implemented for n-GaAs-based Gunn-effect devices by Braslau et al [11], and have been widely used for devices based on III – V compound semiconductors.

Below the AuGe eutectic temperatures of 363°C, inhomogeneous indiffusion of Ge and Ni into GaAs, and some outdiffusion of Ga are observed [12, 13]. They are found concentrated in localized regions of the interface. Also, no major interaction between Au and GaAs was observed. Above eutectic temperatures, typical reactions occurring during alloying are as follows [14-17]:

(i) *'Under-alloy' condition*: Above the eutectic temperatures, Ge diffuses rapidly toward the surface and is trapped by Ni metal layers. A part of Ni diffuses inward into the substrate through the AuGe layer, reacts with As at the interface and forms NiAs. Some traces of Ge and Ga are seen within NiAs regions. Another part of Ni reacts with Ge forming NiGe compounds within the metal layers. While some Au penetrates into the substrate, Ga and As outdiffuse and are found present within NiGe and NiAs phases.

(ii) *Optimum alloy condition*: When alloyed at about 400°C, Ge diffuses into the substrate, where one fraction is captured by NiAs compounds, and another fraction is present at the interface. Ga dissolved in the Ni phases is expelled and Ge from NiGe phases diffuses to the lower NiAs phases. The compound formed had a composition close to $Ni_2GeAs$, or NiAs(Ge). The sizes of the grains have increased compared to the earlier condition.

(iii) *'Over-alloy' condition*: At higher temperatures, the sizes of the grains have increased further. The area at the metal-semiconductor interface occupied by the AuGa phases is increased compared to the above two conditions, and as a result, more Au grains are in contact with GaAs substrate.

Diffused germanium in the form of these compounds acts as a donor and forms a heavily doped $n^{++}$ GaAs layer [18-26]. Ga outdiffusion may affect how Ge dopes the semiconductor [27]. Ge doping in GaAs depends on the population and availability of Ga vacancies, created by selectively gettering a fraction of the cations by gold [12, 28-30]. Increase in contact resistance beyond the critical alloying temperature is related to the saturation of the Au layer with Ga and, also due to excessive As loss [31, 32].

The renowned conducting islet model by Braslau predicted a $(N_D)^{-1}$ dependence of the contact resistance [33-35]. Braslau proposed that current flowed through the Ge-rich islands, which are connected together by the Au overlayer. The real contact area is the hemisphere-shaped region of radius r whose contact resistance $r_c'$ is less than that expected by tunneling. Emission is due to field enhancement at these penetrating points, as shown in figure 1.4. In the Ge-poor regions, the conduction is smaller due to exponential dependence of tunneling current on underlying doping. They are however shorted by Au overlayer and Ge-rich protrusions. Current flow is chiefly through the regions of high conductance [36]. The contact resistance can be measured as

$$r_c = \langle a \rangle^2 \left[ \frac{\rho}{\pi \langle r \rangle} + \frac{r_c'}{2f\pi \langle r \rangle^2} \right] \tag{1.10}$$

where <a> is the mean separation of the protrusions and <r> is the mean radius. $\rho$ is the resistivity of the doped region, f is the field enhancement factor for electron transmission from the protruding electrodes (hemispherical Ge-rich grains of diffusion), which is given as $f >> 1$. For $\rho > 10^{-3}\ \Omega$ cm, the second term in the above relationship can be neglected. Thus, it was proposed that contact resistance was proportional to $\rho$, or alternately, $(N_D)^{-1}$.

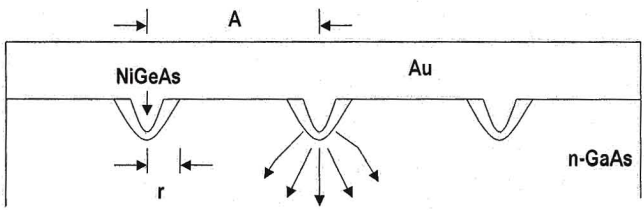


**Figure 1.4. Model of alloyed ohmic contacts to GaAs suggested by N. Braslau [33,34]. Conduction is through a parallel array of Ge-rich protrusions of very low contact resistance.**

HEMT devices have the additional necessity of establishing ohmic contacts to the 2DEG region at the heterointerface of AlGaAs and InGaAs channel layers. The high band gap layer of AlGaAs in HEMT structures poses a barrier to the indiffusion of alloy materials due to strong chemical bonds formed by Al [37]. Heat of formation per bond between Al and As (-1.21eV) is lower compared to that between Ga and As (-0.74eV), making AlAs bonds stronger compared to GaAs bonds [38]. Penetration of

alloy materials through AlGaAs layers is therefore more difficult than through GaAs, has been reported that it requires higher temperatures of alloying [39–41]. However, the role of Ge in doping the Ga vacancies created by Ga outdiffusion remains similar to that of MESFETs [38, 42]. Evidences of phases of $Ni_2GeAs$, NiAs and NiGe in the semiconductor, and Ga outdiffusion into the top metal layers have been presented in the alloyed HEMT device structures, identical to the case of MESFETs [37, 38, 43–46]. It is reported that direct contact to the channel reduces $R_c$ and hence the parasitics, which enables current injection into channel and improves the device performance [38, 47–50]. Excessive outdiffusion of Ga and As, and migration of Ge due to high temperatures deteriorates the contact morphology. This has been minimized with the introduction of a suitable barrier metal like Ag [39, 42, 48, 51], Ti [40], Pt [41, 46], $TiB_2$ [52] and Nb [53], below the overlayer of Au. Refractory NiGe-based ohmic contact materials were also investigated for achieving low resistance contacts [54].

### 1.3. Activation annealing of GaAs

#### 1.3.1. Ion implantation

In an ion implanter, a beam of atoms, usually $Si^+$ or $S^+$ ions for n-type dopants, is generated (ionized) from a gas or solid source by heating or passing a current through the material. Proper ion is selected by adjusting a magnetic field, and the beam is accelerated to kinetic energies ranging from several keV to several MeV, at high voltage in an evacuated tube. These impurity ions are incident on the wafer at the end of the tube in the target chamber and scanned electrostatically over the surface of the wafer. Raster scanning the wafer provides uniform doping of the wafer surface. The ions give up their energy to the GaAs lattice in collisions and finally come to rest at some average penetration depth, called as the *projected range*, $R_p$. The number of ions implanted and their distribution in the GaAs lattice is estimated by the fluency and the energy of the ions. A dose of $\phi$ ions/cm$^2$ is distributed approximately by a Gaussian formula [55]

$$N(x) = \frac{\phi}{\sqrt{2\pi}\Delta R_p} \exp\left[ -\frac{1}{2}\left( \frac{x - R_p}{\Delta R_p} \right)^2 \right] \tag{1.11}$$

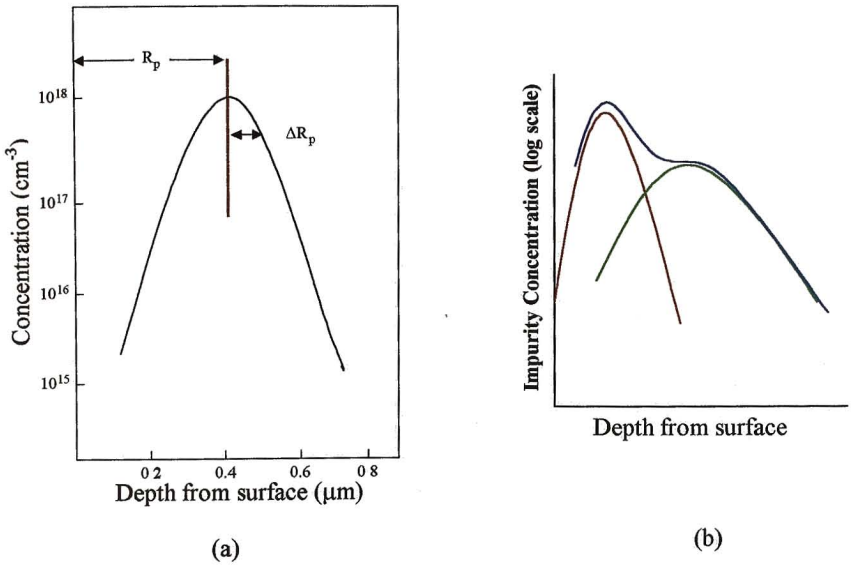


**Figure 1.5. (a) Gaussian distribution of Si implantation in GaAs showing the projected range and straggle. (b) Illustration of a distribution obtained by summing the gaussian profiles of Si implanted at two different energies**

where $\Delta R_p$ is called the *straggle* and measures the half-width of the distribution at $e^{-½}$ of the peak (figure 1.5a). Both $R_p$ and $\Delta R_p$ increase with increasing implantation energy. In order to synthesize a desired profile, several implantations at different energies can be carried out, as shown in figure 1.5b. As the typical energies of implantations needed for GaAs linear devices are 30keV to 200keV, the depth of the peak of the implanted profile is less than 3000Å from the surface of the wafer. The typical doses are $10^{12}$ to $10^{14}$ ions/$cm^2$

Lattice damage results from the collisions between the ions and the lattice atoms [56]. The implanted atoms come to rest at random locations within the material. Most of these damages can be removed by heating after the implantation and also during this treatment, the implanted atoms move into the lattice positions. The process is called *activation annealing*. Dopant atoms become incorporated onto proper lattice sites and supply carriers. About 60% to 95% of the implanted ions are activated, depending on the energy of implantation and amount of dose Doping profile at the interface of active layer and the substrate is not sharp and extends deeper than a Gaussian profile, called as the *'tail'*. This is due to statistics of the implantation and

excess diffusion during annealing. Higher carrier concentration at this region can cause poor device control due to leakage currents.

During implantation, if the implanted atoms enter the open cells that contain no atoms, they travel deep into the crystal in these 'channels' before scattering occurs. This is called as '*channeling*', and results in unpredictable profiles and also increases the concentration of the 'tail' regions [56]. Hence, the wafer is *'tilted'* at an angle to the surface of the wafer during implantation to minimize the effects of channeling [57]. Ion implantation is generally performed with tilts of 10° to 15°.

### 1.3.2. Recrystallization of implanted layers

Amorphization of the GaAs crystals occurs during implantation at room temperatures. Stoichiometric changes produced by forward recoil implantation, and sputtering in the implanted layer influences damage formation. The general depth of damage for low doses of implantations is less than 100nm from the surface.

The activation efficiency is said to improve when the relative magnitude of the Ga–to–As site occupancy of Si is higher, or conversely, when the compensation ratio is smaller [58–60]. Along with the implanted Si atoms, the displaced Ga and As atoms are also present in the interstitials in various forms. Redistribution of these atoms and vacancies occur, and primarily, capture of Ga and As atoms by the respective vacancies takes place to recover the crystalline damage. Stages in rapid solid-state annealing of implantation-amorphized GaAs can be categorized as follows:

(i) At 100-350°C, epitaxial regrowth of the amorphous layer takes place.

(ii) At 350-600°C, implanted acceptor impurities start to become electrically active. Restoration of the lattice to its original state occurs between 400 - 500°C, where increase in resistivity to > $10^7$ Ω/□ is observed.

(iii) At 600-950°C, there is an increase in impurity activation and as a consequence, sheet resistivity ($\rho_{sheet}$) starts lowering [61].

(iv) At 950-1000°C, implanted donor impurities are being activated. It is generally observed that these reactions improve with annealing temperature and time [62, 63]. But, since Si also has amphoteric behaviour, very high temperature and prolonged annealing can result in increase of compensation ratio.

The recrystallization rate of GaAs decreases with increasing implant dose. Recrystallization is completed within the initial 3-5sec of annealing to temperatures of 200-400°C. The secondary defect annealing demands higher processing temperatures in the range of 800-1000°C [61].

### 1.3.3. Electrical activity of the impurities

The electrical activity and diffusion behaviour of impurity atoms are determined by the position they occupy in the III-V semiconductor lattice. Amphoteric group-IV impurities like silicon and germanium, may substitute atoms of both components in semiconductor compounds, and reveal a preference for the larger ones. They behave as donors while occupying the group-III component sublattice, and acceptors in the sublattice of the group-V component. For such impurities, localization of the impurity atom in one or another sublattice is determined by the processing temperature and the vapour pressure of the volatile component at the surface of the wafer. High temperature along with overpressure of group-V components reduces vacancy concentration in the sublattice. Under these conditions, amphoteric impurities preferentially occupy the group-III sublattice substitutionally, where they act as donors. Replacing the group-V component, initiated by this component evaporation, allows the transition to the acceptor state.

Generally, for doses between $10^{12}$ to $10^{13}$ ions/cm$^2$, annealing temperatures about 950°C are necessary for activation. Amphoteric behaviour of Si becomes dominant with temperatures above 950°C. Vacancy formation in the sublattice of group-V component is a factor limiting maximum temperatures. Excess gallium vacancies are created in the near-surface region as a result of sputtering at the surface during implantation, especially with low-energy ions.

The substitutional-interstitial mechanisms of diffusion are being accepted for explaining the impurity behaviour in GaAs. A substitutional impurity is thought to diffuse via jumping from a substitutional site, where it has a high solubility, to an interstitial site where it has high diffusivity. The excess vacancies and interstitials present in the implanted GaAs wafer controls the exchange between the sites.

Vanasupa et al explain the activation mechanism as a two-region process [59]. The initial region is transient when the Si atoms move onto the lattice sites. The second region describes the extent of activation by an equilibrium ratio between Si

donors and acceptors. In this model, activation of Si is assumed as 100% for low concentration, i.e., < $10^{18}cm^{-3}$, and as a monotonically increasing function of temperature. The activation is assumed less than 100% for higher total Si concentrations. The equilibrium equation with neutral vacancies is given by

$$Si_{Ga}^{+} + e^{-} + V_{As}^{0} \leftrightarrow Si_{As}^{-} + h^{+} + V_{Ga}^{0} \tag{1.12}$$

and the compensation ratio assumes the form

$$\frac{\left[Si_{As}^{-}\right]}{\left[Si_{Ga}^{+}\right]} = C(T)\left(\frac{n}{n_i}\right)^{2} \tag{1.13}$$

where C is a constant that varies with temperature. The compensation ratio varies with the square of the electron concentration. Several charged states may be present, but as their estimation and identification is complicated, it is known that the compensation ratio from the equilibrium equations is related to the square of the electron concentration.

For Si concentration of $10^{16}$ – $10^{17}$ atoms/$cm^3$, the electron concentration increases due to the growing number of intrinsic carriers ($n_i$), as a function of temperature. The electron concentration above $10^{17}$ atoms/$cm^3$ is not strongly dependent of the annealing temperature. Si atoms occupy only Ga sites at total Si concentrations below $10^{18}$ atoms/$cm^3$, implying that it acts as a donor [64]. Above this concentration, the amount of Si atoms occupying As sites and neutral pairs increases faster than the amount of Si atoms on Ga sites. Thus concentration dependent diffusion extends deep into the sample and proceeds by diffusion via vacancies in the Ga and As sublattices.

Interaction of interstitial Si atom with neutral vacancies forms active and compensation species with time such as

$$Si_i + V_{Ga}^{0} \rightarrow Si_{Ga}^{+} + e^{-} \tag{1.14}$$

and

$$Si_i + V_{As}^{0} \rightarrow Si_{As}^{-} + h^{+} \tag{1.15}$$

The total Si concentration becomes,

$$\left[Si\right]_{total} = \left[Si_i\right] + \left[Si_{Ga}^{+}\right] + \left[Si_{As}^{-}\right] \tag{1.16}$$

As the concentration of the interstitials become negligible post-activation, we can state that

$$\left[Si_i\right]_{t=\infty} = 0 \tag{1.17}$$

The compensation ratio essentially remains same as the earlier temperature-dependent situation implying that the Si atoms interact with the vacancies in a constant ratio. The rate of activation increases with temperature.

The observation that implanted Si mostly produces n-type doping implies that such a configuration is preferred [64, 65]. Therefore, it is generally accepted that the population of Ga vacancies predominantly governs diffusion of Si [65]. There is some optimum concentration of vacant sites beyond which the effect of compensation, most probably by ionised point defects and/or their complexes with the existing dopant atoms, starts to predominate [65].

### 1.4. Rapid thermal processing

Rapid thermal processing (RTP) uses incoherent radiation from tungsten halogen lamps as the source of energy for activation annealing and contact alloying processes. One of the major advantages of RTP is due to the availability of expanded time regimes (to shorter times). Short time processing reduces the anneal time-temperature product (thermal budget) such that the desired physical or chemical processes are accomplished and the unwanted ones are made less probable, especially in partially fabricated structures [66]. In an RTP, the spectrum of emission from the lamps consists of radiation from the vacuum ultraviolet (VUV) to the IR regions. RTP uses both the photo effects of radiation in VUV/ visible spectrum and the IR radiation, and the features of high heating and cooling rates [67]. Hence, the efficiency and throughput of RTP is very high.

In RTP, maximum heat is incident and transferred to the wafer placed within a quartz chamber. Typically, the wafer is held by quartz pins and is thermally isolated. The thermal mass thus being very low aids a rapid temperature rise. Steep thermal gradients across a wafer during the rapid heating or cooling phases induce slip lines at the periphery of the wafer [62, 68, 69]. During the cooling phase, edge of the wafer radiates faster compared to the center of the wafer. Slip formation is minimized by careful design of the ramp up and ramp down rates, and also by using a graphite susceptor. A susceptor behaves like a blackbody structure and also as an extension of the wafer [69]. Ramp up rates are generally limited by the ability of silicon nitride encapsulation in prevention of arsenic out-diffusion. Thermal uniformity is also

etermined by gas flow rates due to transfer of heat between the ambience and the wafer.

### 1.4.1. Rapid thermal annealing

Halogen lamp annealing of GaAs was first reported by Arai et al [70]. Annealing generally performed about 950°C in an RTP leads to good activation of Si [71]. The peak temperature of the anneal cycle required to provide optimum electrical activation increases with implanted dose [72]. For higher energies, higher activation and mobilities are possible to be obtained, as well as tighter spreads of dopant profiles [73]. Activation is lower for lower implant energies [62]. With improvements in activation, the resulting higher carrier concentration of the $n^+$ region yields a lower contact resistance [73]. A sharp and abrupt 'tail' in the channel carrier concentration results in higher transconductances as well as lower pinch-off voltages of the MESFETs [74, 75].

### 1.4.2. Rapid thermal alloying

RTP alloyed contacts have been known to have 30-50% lower contact resistances and better uniformity compared to furnace alloying [69, 76]. S. S. Gill et al first introduced alloying by IR lamps using production activation annealing equipment for n-GaAs for AuGe-based [77] and AuGe/Ni-based ohmic contacts [78]. While alloying is generally performed above the melting point of AuGe eutectic alloy, higher temperatures upto 500°C are resorted to depending on the thicknesses of the multilayers of metallisation, ramp rates and device layers. Fine-grained microstructures consisting of uniformly distributed Ge-rich and Au-rich phases are being routinely achieved by RTA alloying [79].

## 1.5. Characterization

### 1.5.1. Contact resistance

The basic physical model for obtaining contact resistance assumes that an electrically conductive semiconductor layer is situated between an insulating substrate and an ohmic contact. This conducting layer is assumed to be thin with respect to the lateral width of the metallisation (assumed semi-infinite). A resistance is associated with current flow between the conductive layer and the metallisation. The material

under the contact is characterized by the bulk resistivity, ρ, and the transition between the bulk materials and the ohmic contact is characterized by specific contact resistance, $r_c$. Further, the sheet resistance of the material below the pads, and that of the GaAs material between the metal pads will not be same due to reactions during alloying. They are named as $R_{sh1}$ and $R_{sh2}$, respectively.

The widely used practical test structure consists of differently spaced ohmic contacts, as illustrated in figure 1.6. The technique is known as *transfer length method* (TLM), and adopts more than three pads of width W [80]. The pattern is isolated to restrict current flow only across the separation between pads, L. The resistance between two adjacent pads is composed of the two contact resistances $R_c$ plus the resistance of the semiconductor layer between them. The resistance of the semiconductor region is dependent on the sheet resistance of the semiconductor, width of the contact and the spacing, L. Figure 1.7 shows a slab of semiconductor material with a cross-sectional area A, length L and an ohmic contact covering each end of the material slab. If ρ is the resistivity of the semiconductor, the resistance from end to end is given by

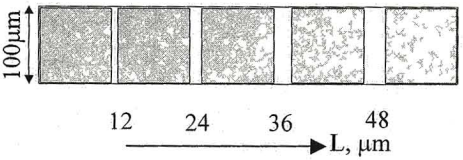


**Figure 1.6. Schematic of a TLM structure**

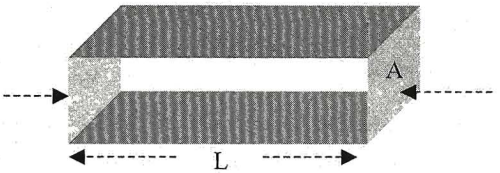


**Figure 1.7. A slab of semiconductor with ohmic contacts on the two ends.**

$$\rho\frac{L}{A} \tag{1.18}$$

Hence, the total resistance is

$$R = 2R_c + \frac{\rho}{Wt}L \tag{1.19}$$

or,

$$R = 2R_c + \frac{R_{sh2}}{W}L \tag{1.20}$$

This has the form of the equation of a straight line and therefore, assuming that the sheet resistance is constant, a plot of measured resistance as a function of spacing will yield a straight line, as shown in figure 1.8. Then, from the y-intercept and slope, we can determine quantities of

$$R_c = \left(\frac{1}{2}\right) \times Intercept \tag{1.21}$$

and,

$$R_{sh2} = R_s = (W \times Slope) \tag{1.22}$$

The transfer length method, thus, completely characterizes the contact by providing the sheet resistance, the contact resistance, and the specific contact resistance. The contact resistance $R_c$, thus determined experimentally, is normalized to the width of the pads and given in Ω-mm, due to its practical significance.

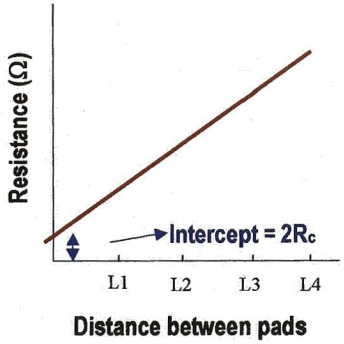


**Figure 1.8. Plot of measured resistance as a function of contact separation using the TLM pattern.**

### 1.5.2. D. C. Characterization

During MESFET operation, for sufficiently large $V_D$, at some critical electric field, the current will saturate at a value $I_{dsat}$ or $I_{sat}$, called as *saturation current*. The carriers attain velocity saturation. The voltage at which the current changes from linear to saturated region is called the

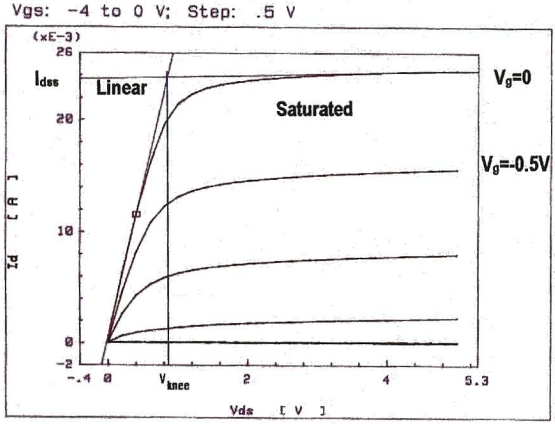


**Figure 1.9. Typical I-V characteristics of a MESFET with negative gate bias.**

*saturation voltage*, $V_{sat}$. After gate formation, $V_{sat}$ is measured as *knee voltage* ($V_{knee}$)

in the I-V characteristics, and is defined similarly. This is an important figure of merit and is a sign of optimum alloying.

The basic current-voltage (I-V) characteristics of a MESFET are illustrated in figure 1.9. The gate voltage at which the channel is completely depleted of carriers is known as the *pinch-off voltage*, $V_p$. Representing the change in $I_{ds}$ as a function of $V_g$, *transconductance* ($g_m$) is defined for a fixed gate voltage step as

$$g_m = \frac{dI_{ds}}{dV_g} \tag{1.23}$$

The apparent value of these quantities is altered by the presence of resistance (of even 1ohm) on the source side of the device, called as '*source resistance*', $R_s$. Source-drain current flows through the device as well as through this resistance. This reduces $I_{dss}$ and $g_m$. If $g_{me}$ and $g_{mi}$ are defined as external and intrinsic transconductances (with and without $R_s$), respectively, then,

$$g_{me} = dI/dV_e \tag{1.24}$$

$$g_{mi} = dI/dV_i \tag{1.25}$$

$$V_e = V_i + IR_s \tag{1.26}$$

The intrinsic transconductance can then be rewritten as

$$g_{mi} = \frac{g_{me}}{1 - g_{me}R_s} \tag{1.27}$$

If $I_i$ represents the current with $R_s$=0, $I_e$ the current with $R_s \neq 0$, then

$$I_i = I_e(1 + g_{mi}R_s) \tag{1.28}$$

The parasitic resistances are defined as follows: The *source resistance*, $R_s$, is the resistance between the source metal and the gate. This includes the contact resistance of the source. Similarly, the *drain resistance*, $R_d$, is the resistance between the drain metal and the gate. These are also known as the *access resistances* and are extracted by involved measurements and calculations [5]. These resistances introduce an IR drop between the gate and the source and drain contacts [1].

### 1.5.3. R. F. Characterization

One of the basic modes of operation of MESFETs is the common-source configuration. The RF input is applied between the gate and source, and the RF output is derived between the drain and source terminals. The device is dc biased. The RF characteristics are obtained by measuring its scattering parameters or S-parameters

[5]. S-parameters are most easily measured at microwave frequencies [4]. The parameter $S_{21}$ represents the *RF gain* of the device expressed in units of dB.

The *RF transconductance*, an extracted RF parameter, can be generally defined as an addition of the value of DC transconductance to the effect of parasitics of the FET, in the presence of an AC signal value. This signifies the influence on the RF gain or amplification performance of the FET.

Another important figure of merit describing the device is the *cutoff frequency*, $f_t$, and defined as

$$f_t = \frac{g_m}{2\pi C_{gs}} \tag{1.29}$$

where $C_{gs}$ is the capacitance of the depletion region between the gate and source. Useful gain from a device can be obtained only at frequencies well below $f_t$, but the higher is $f_t$, the higher is the gain of the device at any lower frequency, f.

### 1.5.4. Thermal Imaging

In order to obtain reliability data from accelerated temperature testing, knowledge of temperature of the hot zones of the device or the MMIC is fundamental. Devices like FETs and resistors are significantly hotter than the surrounding areas. The chemical or physical changes that lead to failure often occur in these areas. The individual elements of MMICs are appreciably hotter than nearby areas of the chip as the active regions are very small and also since GaAs is a poor thermal conductor compared to Si. This is normally higher than the ambient or baseplate temperature. The rise in temperature is characterized by the thermal impedance of the device. Thermal impedance or thermal resistance is defined as the difference between the temperature of the hottest region and the baseplate or ambient reference temperature divided by power input to the device, or the part of the chip of interest. This varies with device size and thickness. When $T_b$ is the baseplate temperature, $\theta$ is the thermal resistance, and P is the dissipated power (current x voltage), then the temperature of the active layers of the device $T_c$ is given by [9]

$$T_c = T_b + \theta P \tag{1.30}$$

There are three common methods used to measure temperature on GaAs devices. They are infrared microscope, liquid crystal and electrical diode drop [9, 81, 82]. The IR microscope is the most convenient technique to obtain temperature profile

data [9]. In the infrared microscope, IR emission from the surface of the chip is focused by the microscope onto an IR sensor, and the temperature is determined. The emissivity of the surface is determined using computerized commercial instruments in a procedure in which the IR radiance is recorded at several temperatures while the overall device is heated, but unpowered. The instrument subsequently uses this calibration when power is applied to the device. This equipment produces pixel-by-pixel maps of temperature over the surface of the powered chip. With a limitation of spatial resolution to about 15μm, temperature can be measured with accuracy of 1°C. Thermal modeling software, mostly developed for the individual thermal imaging system, is used to understand and produce a map of the peak temperature zones and the surrounding less hotter areas of the chip.

### 1.5.5. Accelerated thermal aging

Devices in high performance military and space applications are expected to function as intended over some reasonable lifetime and under imperfect environmental conditions. The chips are always vulnerable to chemical and physical changes that occur within the constituent materials of the device itself even if they are passivated and packaged. Electrical current flow, and operating temperatures often increase the rates of these changes. Sudden loss of functionality is addressed as *catastrophic failure*, and a gradual degradation in performance is called as a *soft or graceful failure*. Stipulated tests such as accelerated thermal aging, thermal aging under electrical stress, radiation hardness, etc., are mandatory for use in strategic applications.

For GaAs devices, contact metallisation related failures are known to be considerable, especially in submicrometer devices. Hence, thermal stability, limited metal diffusion, good edge definition and good heat dissipation are advantageous. In these devices, the typical current densities and the temperatures throughout the metal film and contact window can be greater than $10^5$ A/cm$^2$ and 150°C, respectively [8]. The electric field between electrodes is also large due to very narrow spacings between various electrodes. With such conditions of high current density, high temperature, and high electric field, contact failure mechanisms can be grouped into three categories, viz., (i) degradation due to interdiffusion between metallisation and semiconductor, (ii) metallisation shorts or open circuits due to electromigration along

narrow conductors carrying large current, and (iii) interelectrode shorts due to the field induced electrode material transport [8].

When we consider the temperature-accelerated failure, the reaction rate R at which a failure process (or chemical and physical changes) proceeds is described by the well-known Arrhenius equation [5]

$$R = R_0 \exp\left(\frac{-E_a}{kT}\right) \tag{1.31}$$

where R is the reaction rate, $E_a$ is the activation energy of the process in eV, $R_0$ is the pre-exponential constant, k is the Boltzmann constant (8.616 x $10^{-5}$ eV/K), and T is the absolute temperature in K. The exponential dependence on temperature can generate failures by testing at elevated temperatures, and thereby experimentally establishing reliability data in an appreciable time period. When the elevated temperature aging process, proceeding at a reaction rate R, results in some degradation mechanism, contact failure occurs after time t, where

$$t = \frac{1}{R} \tag{1.32}$$

when the reaction is assumed to proceed linearly in time. From Arrhenius equation, we obtain:

$$t = \left(\frac{1}{R_0}\right)\exp\left(\frac{E_a}{kT}\right) \tag{1.33}$$

In the present context, failure criterion of contacts can be defined as the amount of drift in the contact resistance value by a certain factor occurring due to the degradation mechanism. Then, the natural logarithm of the failure time $t_F$, is given as

$$\ln(t_F) = A + \left(\frac{E_a}{kT}\right) \tag{1.34}$$

where A is a constant. Failure time is determined at different temperatures. Thus, assuming that contact degradation is due to a single failure mechanism, the plot of natural logarithm of the failure time against the inverse of absolute temperature results in a straight line. This line, when extrapolated to the operating temperature of the contact, helps determining the lifetime of the contact at that operating temperature [83]. For example, the life at 110°C and 125°C, required for typical flight applications, can also be estimated with reasonable approximation. This also allows experimental determination of the activation energy of the process. *Activation energy* is a measure of how effectively a reaction uses thermal energy. It measures how

rapidly mean lifetime changes with temperature. The higher the activation energy, the greater the accelerating effect of temperature.

In practice, even an occurrence of a drift of at least +20% in the value of $R_c$ as a failure criterion does not cause any appreciable change in the RF characteristics of MESFET [84]. Aging at different temperatures with a step of about 20°C is generally preferred to provide sufficient stress levels in order to give rise to appreciable differences in failure times for calculation of activation energies [85]. The general failure mechanism observed in ohmic contacts is due to the excessive interdiffusion of Ga and Au [86, 87]. Contacts also have shown degradation owing to 'under-alloying' [88]. As a result of changes in $R_c$, large drifts in electrical characteristics like $g_m$, source and drain resistances, etc., have affected the device performance [88, 89]. Therefore, contacts showing minimal drift during performance would ensure a long life of the devices.

### 1.5.6. Diffusion

Diffusion describes the process by which impurity atoms move in a crystal lattice. In addition to concentration gradient and temperature, crystal structure and defect concentration also play a major part in this process.

In *substitutional diffusion*, the impurity atom wanders through the crystal by jumping from one lattice site to the next, thus substituting for the original host atom

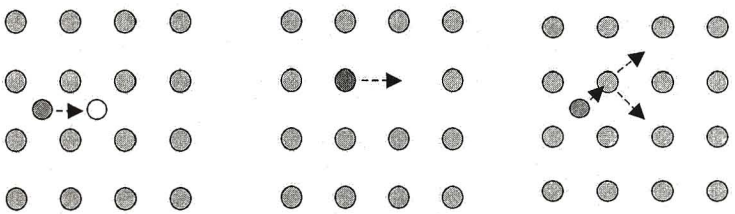

**Figure 1.10. Examples of diffusion mechanisms: (a) interstitial diffusion, (b) vacancy mechanism and (c) substitutional or kick-out mechanism**

(figure 1.10). However, it is necessary that the adjacent site needs to be vacant, or, vacancies must be present to allow substitutional diffusion to occur. In *interstitial diffusion*, an impurity atom moves through the crystal lattice by jumping from one interstitial site to the next. This process is relatively fast due to the large number of

vacant sites of this type in a semiconductor. The modified version of the substitutional diffusion is the *interstitialcy diffusion.* Here, interstitial host atoms (self-interstitials) are annihilated by pushing substitutionally located impurity atoms into these interstitial sites. These impurities can now diffuse to adjacent substitutional sites and create new self-interstitials. Thus, the interstitial position of the diffusing impurity atom is purely a transition state, in moving from one substitutional site to the other.

Fick's second law describes diffusion. If we consider the flow of particles in a crystal of cross-section A, between planes P1 and P2 separated by dx, the rate of accumulation of particles in this region is described in one dimension by the equation

$$\frac{\partial C}{\partial t} = \frac{\partial}{\partial x}\left(D\frac{\partial C}{\partial x}\right) \tag{1.35}$$

and for the three-dimensional case it is

$$\frac{\partial C}{\partial t} = -\vec{\nabla}\cdot\vec{J} \tag{1.36}$$

where J is the flux which is concentration C times the velocity v. D is the diffusivity or diffusion coefficient given by

$$D = D_0 \exp\left(\frac{-E_a}{kT}\right) \tag{1.37}$$

where $D_0$ is the diffusion constant, and the minus sign appears because the flux is in the direction of decreasing concentration. In majority of cases, the problem of interest is a determination of the diffusion profile for a diffusion of species whose concentration in the host crystal is initially zero. The diffusion profile will depend on the initial and boundary conditions. When the diffusion coefficient is constant, the diffusion equation in one dimension is

$$\frac{\partial C}{\partial t} = D\left(\frac{\partial^2 C}{\partial x^2}\right) \tag{1.38}$$

Two different solutions to the above equation are frequently encountered. These are designated by the boundary conditions. The first is the case for an infinite source that maintains a constant concentration at the sample surface during the diffusion, and the second is where the total amount of the diffusing species is fixed, i.e., when a thin layer of impurity atoms is deposited on the GaAs wafer, and used as the diffusion source. In either case, the sample is generally of sufficient thickness to require only consideration of diffusion from one surface.

In diffusion from an unlimited source (constant-surface concentration) when a wafer is exposed to an infinite amount of the impurity during the diffusion period, the concentration is described by the complimentary error function.

For a limited source diffusion, the solution that satisfies the conditions is

$$C(x,t) = \frac{Q}{(\pi Dt)^{\frac{1}{2}}} \exp\left(\frac{-x^2}{4Dt}\right) \tag{1.39}$$

where Q is the amount of dopant deposited at the wafer surface, D is the diffusivity at the specific temperature, C(x, t) is the concentration of the dopant as a function of depth x and time t. This solution is the well-known Gaussian and the equation is often called as the *Gaussian distribution function diffusion equation.* The diffusion condition is referred to as the predeposition from a thin layer source or drive-in diffusion from a fixed total dopant concentration. The area under the curve always remains constant, which is the total amount of impurity present. Both solutions are based on classical diffusion theory for diffusion into a semi-infinite slab, and are a reasonable approximation for typical shallow diffusions into semiconductors [90]. Although the diffusants may not be ideal, the solutions to Fick's second law can be used to estimate the doping profiles for practical diffusions. Experimentally, the diffusivity is obtained by fitting the above equation to the experimental diffusion profile [64, 91].

### 1.6. Motivation and objectives for present work

MESFETs and pHEMTs are used in MMICs being manufactured in Gallium Arsenide Enabling Technology Centre, (GAETEC), Hyderabad. These MMICs are used in high performance, challenging conditions in strategic applications for which thermally stable and reliable ohmic contacts are crucial. Formation of low resistance ohmic contacts to MESFETs and pseudomorphic HEMTs are necessary for efficient device operation. In order to obtain very low values of ohmic contact resistance, it was necessary to study in detail the electrical properties and material structure of ohmic contacts to MESFETs and pHEMTs. Investigations were carried out to understand the role of processing parameters on ohmic contacts through extensive material and electrical characterization. The thermal stability of ohmic contacts and influence of silicon implant activation on ohmic contacts were also studied.

The various aspects studied are described below:

MESFETs:

1. A high doping concentration at the metal-$n^+$-GaAs interface is responsible for producing low resistance ohmic contacts, as discussed in § 1.2.1 and 1.2.2. [8, 9, 54, 92, 93]. However, even with higher concentration at the interface formed after alloying, low contact resistances could not be achieved. Therefore, this could be only a necessary but not sufficient condition. Hence, it was essential to investigate the critical conditions of low resistance contact formation.
2. The surface morphology of low resistance contacts is reported to be rough [5]. It is reported in the literature that with increase in alloying temperature the contact resistance reduces, but at the same time surface roughness increases. We have investigated whether it is possible to obtain low resistance contacts with lower surface roughness.
3. Post-implantation annealing is performed to activate the implanted silicon ions for obtaining desired doping levels in the channel as well as in the contact layers. The role of activation of the channel layer in assisting low resistance contact formation was also studied.

Pseudomorphic HEMTs:

1. Direct contact to the channel has been believed to reduce the contact resistance and improve the performance of pHEMTs [38, 47–50], as discussed in § 1.2.1. Additionally, it has been reported that penetration of alloy elements through AlGaAs layers requires temperatures as high as 430°C or above [39–41]. The importance of alloying temperature on contact resistance reduction is addressed.

### 1.7. Thesis plan

This introduction chapter briefly described MESFETs and pHEMTs used in MMICs. An account of the literature survey on ohmic contacts, ohmic contact theory, activation annealing were presented to obtain directions to the present study.

The following chapters describe the experiments carried out and the results of the characterization and conclusions derived from the studies.

Chapter II describes the experimental details of contact alloying of MESFETs and pHEMTs, rapid thermal annealing experiments, experimental facilities and conditions utilized. Specimen preparation technique for cross-section transmission electron microscopy (XTEM) studies has been described.

Chapter III presents the results of the alloying experiments on MESFETs. Detailed characterization techniques such as SIMS, TEM, SEM, AFM, and electrical device performance were used to comprehend the low resistance contact formation and surface morphology. Optimum contact formation is discussed. This chapter also discusses the aspects of contact stability and reliability.

Chapter IV discusses the influence of activation annealing on ohmic contact formation. Rapid thermal annealing experiments were carried out to improve activation of silicon implanted device layers. Various material and electrical characterization techniques such as SIMS, C-V profiling, etc., were used to understand activation behaviour and its influence on low resistance ohmic contacts. The results are discussed.

Chapter V discusses the contact formation approach to pseudomorphic HEMTs. Characterization techniques such as SIMS, TEM, SEM and AFM were used to examine the results of alloying conditions and the role of AlGaAs layers. Optimum contact formation and current flow path are discussed.

Chapter VI summarizes the results of studies of ohmic contacts to MESFETs and pHEMTs. Important conclusions of low resistance contact formation are listed. Scope for future work is also presented.

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# Chapter II

## Experimental Details

*This chapter presents the details of the fabrication of MMICs, annealing and alloying experiments, sample preparation techniques for cross-section TEM, and various experimental techniques used during the study. Rapid thermal processor, thermal evaporation, and other systems used during the experiments and characterization are described.*

### 2.1. Ion implantation

Ion implantation was carried out at GAETEC, Hyderabad, in an Eaton NV-6200A system (figure 2.1). This was a medium current, cassette-to-cassette production machine capable of handling 3" diameter wafers. The operating energies were ranging from 5keV to 200keV, with a uniformity ($\sigma$) of dose less than 0.5% over a wafer The system had a 90°, double focusing magnet for analysis of the primary ion beam The beam monitor and control section had a CRT circuit for setup of beam, where with the digital scan system, the beam was optimally focused. Silicon ions ($Si^{29+}$) were implanted for obtaining the active layers.

**Figure 2.1. NV6200A ion implanter**

Semi-insulating (S. I.) GaAs wafers used for this study were single-side polished. Wafers were ion implanted with doses of 6 x $10^{12}$ $cm^{-2}$ at 180keV followed by 1.5 x $10^{13}$ $cm^{-2}$ at 35keV, for obtaining the channel and contact layers. Additionally, wafers implanted with 7 x $10^{12}$ $cm^{-2}$ and 2.5 x $10^{13}$ $cm^{-2}$, respectively, were used for studying the effect of increased concentration on contact resistance Tilt of the wafers during implantation was 10°

### 2.2. Rapid thermal processor

The activation annealing and contact alloying experiments were carried out in the AET Thermal RXV6 rapid thermal processor (RTP) system (figure 2.2). In this

system, 24 high power quartz halogen lamps in an infrared reflective gold plated enclosure, housing a quartz chamber, provided very fast ramp-up rates. The cooling rates were aided by multiple compressed cold air-cooling and hot air extraction. The system had computer-controlled closed loop temperature control with type K thermocouples. One thermocouple handled the closed-loop temperature control and monitored the temperature, and the other performed uniformity control in real time.

**Figure 2.2. RXV6 Rapid thermal processor**

The gases for providing inert atmosphere during annealing or for purging purposes, such as, nitrogen and hydrogen, were filtered and delivered through individual mass flow controllers. Nitrogen was used during activation annealing. A vacuum pump, providing vacuum down to $10^{-3}$ Torr, was used to pump down the chamber before, during, or after the temperature cycle to achieve environment control

The wafers were placed on a graphite susceptor held by a quartz tray. The susceptor had recessed slots to match the wafer dimensions so that heat transfer was effective during heating as well as cooling.

When the process cycle was executed, the system achieved the desired temperature in seconds due to fast ramp up rates In the present experiments, ramp up rates of about 30°C/sec were applied to raise the temperature from ambient to the required annealing temperatures. A typical RTA

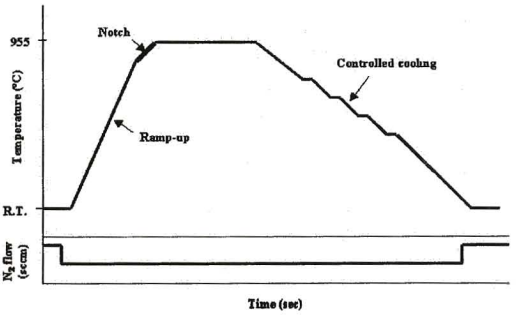


**Figure 2.3. The typical annealing profile of RTA with the ambient gas flow cycle. The ramp down phase is tailored to control the cooling phase, and a notch is introduced to prevent any overshoot.**

cycle is illustrated in figure 2.3. A 'notch' at the end of the ramp up of temperature was set to avoid any overshoot of temperature. The ramp up rate was intentionally slowed to rates less than 5°C/sec from 30°C/sec at this point. The cooling phase was programmed to follow a slower rate to reduce slip formation [1]. This controlled cooling step allowed the center of the wafer to cool at a nearly same rate as that of the periphery of the wafer. The lamps were not entirely turned off in this condition. For temperatures below 900°C, the temperatures were held for a few seconds at intervals of 100°C till the ramp down temperature reached 500°C, as shown in figure 2.3. Hence, steep temperature gradients were not allowed to occur. A controlled gas flow at 1000sccm was maintained during annealing. Activation annealing experiments were performed between 925°C and 955°C at a fixed time of 15 sec, and at 945°C and 955°C for different anneal times to determine the lowest sheet resistivity ($\rho_{sheet}$).

During contact alloying a mixture of nitrogen and hydrogen (forming gas) was used as the ambient gas, with 2000sccm and 500sccm flow rates, respectively. The ramp up rates during alloying were about 50°C/sec. Alloying experiments on MESFETs were done between 380°C-420°C, at a fixed time of 150 seconds, and at 390°C and 400°C for different alloying times for achieving the lowest contact resistance ($R_c$). To understand the effect of different alloying durations on the electrical parameters at higher temperatures above 400°C, experiments for different alloying times were also performed at 410°C and 420°C. On pseudomorphic HEMTs, experiments were performed between 390°C and 450°C for 45sec, and at 430°C for 30 sec and 60sec to obtain low contact resistances.

### 2.3. Ohmic metallisation

Ohmic metallisation was carried out in a thermal evaporation system. The system used during the experiments was a mid-volume, batch-type deposition system from CVC products, Inc., Rochester, NY, USA, model no. SC-4500 (figure 2 4).

The unit contained a vacuum chamber with an 18" diameter steel bell jar, pumped by a high vacuum cryo pump and backed by a mechanical pump. After

**Figure 2.4. SC-4500 thermal evaporation system**

reaching high vacuum, pumping continued for about 2 hours until a pressure of at least 1 x $10^{-7}$ Torr before starting deposition. Inficon IC/4 controller was used for measurement of thickness of deposited material.

AuGe, Ni and Au materials were weighed to about 1.6, 1.5 and 4.2 gms., respectively, as per required thickness and placed in individual alumina crucibles that were held by tungsten filaments. Wafers were mounted on the substrate holder, which was rotated during deposition. Vacuum during deposition was maintained at 1 x $10^{-6}$ Torr. The current during deposition was about 12-16A. The deposition time was varying between 8 to 20 min, for different layers.

### 2.4. Fabrication of MMICs

The structures of MESFET and pHEMT, and fabrication details of MMICs are briefly described. They were fabricated using the standard MESFET and pHEMT processes of GAETEC, Hyderabad [2].

#### 2.4.1. Structure of MESFETs

After implantation, the wafers were next treated in oxygen plasma for 7 min in March Plasmod plasma etcher, model # GCM-200 using 25 W RF power with 2 sccm flow rate of $O_2$ [3]. Silicon nitride film of thickness about 550Å with a compressive stress was deposited using a Plasmatherm Plasma Enhanced Chemical Vapour Deposition (PECVD) system. After annealing, the nitride films were removed in buffered hydrofluoric acid and their sheet resistivity was measured using Biorad HL 5500 Hall measurement system. The concentrations of the $n^+$ and channel layers were 2 - 3 x $10^{18}cm^{-3}$ and 2 - 3 x $10^{17}cm^{-3}$, respectively. The typical layer thicknesses were about 0.15μm and 0.30 - 0.35μm, respectively. Figure 2.5 shows a typical structure of a MESFET.

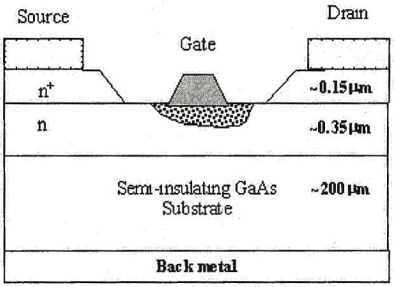


**Figure 2.5. A typical structure of MESFET indicating the source-drain contacts and the recessed gate.**

#### 2.4.2. Structure of pHEMTs

The typical pHEMT structure, grown by molecular beam epitaxy (MBE) technique, is shown in figure 2.6. 3" wafers with the pHEMT epitaxial structure were

grown at MBE Tech, Singapore. The thickness of different layers were as follows: superlattice buffer, consisting of 10 periods of alternate layers of undoped $Al_xGa_{1-x}As$ (x=0.24) and undoped GaAs, each with a thickness of 50 Å; S. I. GaAs buffer layer: 5000Å; $In_xGa_{1-x}As$ (x=0.15) channel: 120 Å; $Al_xGa_{1-x}As$ (x =0.24) spacer layer: 30 Å; a Si δ-doped layer with 6 x $10^{12}cm^{-2}$; $Al_xGa_{1-x}As$ (x = 0.24) Schottky layer: 250 Å, and $n^+$-GaAs contact layer: 500 Å, with a concentration of 5 x $10^{18}cm^{-3}$.

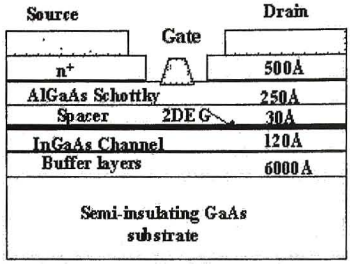


Figure 2.6. A typical schematic of a pHEMT device structure.

### 2.4.3. Fabrication

Mesas were formed by photolithography, and the wafers were etched using $H_2SO_4$:$H_2O_2$:$H_2O$::1:1:100, for a duration of about 7.30 min. The breakdown voltages were measured to ascertain the completion of mesa etching.

Next, source-drain pads were opened on the mesas. Wafers were treated in HCl:$H_2O$::1:1 for 5 min to remove any leftover scum layer. AuGe/Ni/Au (1000 Å/300 Å /3000 Å) ohmic metal layers were then deposited by thermal evaporation. The metallisation from the unwanted regions of the wafers were then lifted-off. The wafers were next rapid thermal alloyed in forming gas environment. DC measurements on TLM, FETs, mesa resistors and mesa isolation structures, were measured immediately after alloying. The source-drain currents measured at this stage served as the reference during the gate recess etching.

Then, gate patterns were opened with gate lengths of 0.5μm or 0.7μm. During recess etching, the $n^+$ layers inside these openings were etched completely. Simultaneously, openings for the bottom electrode of the capacitor, and underpasses were formed. Ti/Pt/Au (600 Å/300 Å/4500 Å) gate metallisation was done by e-beam evaporation on those openings. After lift-off, various DC parameters were measured.

A silicon nitride dielectric film was deposited by PECVD. This layer was also used as the dielectric film for the capacitors. A polyimide layer, to form low-value capacitors, was spun on the wafers and cured at about 330°C.

Interconnects were formed by sputtering followed by selective area electrodeposition. First, Ti/Au seed layers (500 Å /1000 Å) were sputtered. After patterning, the wafers were electroplated with gold to a thickness of 2.5μm.

During processing, thickness of different metallisation and mesa height were measured by Dektak surface profiler. Sheet resistivity of the metallisations was measured using M-Gage of Tencor Instruments.

The wafers were finally passivated with a thicker film of silicon nitride This completed the front side processing.

The backside of the wafers was thinned to 100μm or 200μm, depending on the performance requirements. Ti/Au films (500 Å /3000 Å) were then sputtered and further electroplated with gold (~5μm), to serve as the back metal as well as the ground plane for the microstrip components in the MMIC. The wafers were finally DC characterized.

On-wafer RF characterization was performed to obtain cut-off frequency and other s-parameters of the individual FETs. MMICs were then diced and assembled on Au-plated kovar or CuW metal carriers, or suitable packages along with necessary passive components for characterization of the individual circuits.

## 2.5. Characterization

In this section details of the characterization facilities and techniques are presented.

### 2.5.1. Electrical measurements

The wafers were DC characterized using HP 4142B DC source attached to a Signatone DC prober. A separate area of each tile in a wafer, known as *process control monitor* (PCM), contained representative active and passive devices, where all the electrical characterization was carried out during processing (figure 2.7). After alloying, the contact resistance ($R_c$) measurements were carried out on TLM structures. Parameters such as source-drain current ($I_{ds}$) at different gate voltages ($V_G$), knee voltage ($V_{knee}$), and

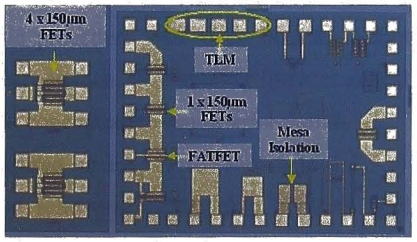


**Figure 2.7. A process control monitor (PCM) showing important devices.**

transconductance ($g_m$) were measured after gate metallisation on 1 x 150 μm MESFETs. C-V profiling performed on FETs with a large gate length (20μm), known as *FATFETs*, were used to extract the profile of doping concentration in the channel. Final DC and RF measurements were done on 4 x 150μm MESFETs. RF measurements such as the S-parameters were carried out using HP8720C VNA, and the power measurements using HP83752 Synthesizer and R&S NRVS power meter. The extracted RF parameters such as RF transconductance were obtained through the standard programs used for model parameter extraction at GAETEC [2].

### 2.5.2. Hall measurements

Hall measurements were carried out using the van der Pauw technique [4] to measure the carrier concentration, resistivity and mobility at a given temperature. During this work, an S-110 Keithley Hall measurement system was used to obtain the mobility values. Samples from individual wafers were cut to a typical size of 1-2 $cm^2$. The four corners of these samples were made ohmic by fusing indium, and soldered into the sample holder for measurements.

### 2.5.3. Capacitance-voltage profiling

Electrochemical C-V profiling was carried out in Biorad C-V profiler using an electrolyte solution to form the Schottky contact. Under specified conditions, the electrolyte etched into the active layers, allowing continuous measurement of capacitance. The electrolyte was present within a cell with a small, circular orifice to define the Schottky diode area. The basic procedure was to dc bias the Schottky barrier to produce a depletion depth and capacitance. Wafers after implant annealing were C-V profiled to obtain the activated Si concentration-depth information.

The doping profile were also measured on FATFETs (shown in § 2.5.1) by forming a Schottky diode, and using the following relationship between applied voltage and diode capacitance:

$$N(x) = \frac{2}{q\varepsilon A^2}\left\{\frac{-1}{d\left(1/C^2(x)\right)/dV}\right\} \qquad (2.1)$$

where N is the doping concentration, q is the electron charge, ε is the permittivity, A is the diode (metal plate) area, C is the capacitance, and V is the applied voltage. The depth x was obtained from [5]

$$x = \varepsilon A / C \qquad (2.2)$$

The electrical or FATFET C-V profiling was performed to extract the concentration-depth profile of the channel layer.

### 2.5.4. Secondary Ion Mass Spectrometry (SIMS)

SIMS was used to measure the impurity profiles in GaAs after implant activation of silicon. SIMS was also used to obtain the diffusion profiles of ohmic contacts.

Heavy primary ions (oxygen or cesium) with energies between 1 and 20 keV is used to sputter the sample, and transfer the energy to atoms in the surface through direct or indirect collisions. This creates a mixing zone consisting of primary ions and displaced atoms from the sample [6]. The resulting secondary ions are then analyzed using a mass spectrometer. The primary ion beam continuously sputters the sample, advancing the mixing zone into the sample and creating a sputtered crater. Flat-bottomed craters are formed by rastering the ion beam over an extended area. Stray ions from the crater walls (other depths) are rejected and only secondary ions from the central, flat-bottomed region of the crater are collected.

SIMS analyses were carried out using a Cameca system at M/s Charles Evans & Associates, Sunnyvale, CA, USA. Cs primary ion beams with primary ion energy of 14.5keV were used to monitor Si on the samples activated after ion implantation. The analysis craters formed due to rastering of the primary beams were depth profiled using a stylus profilometer. The detection limits of C and Si were 1 x $10^{16}$ and 1 x $10^{14}$ atoms/cm$^3$, respectively.

For the analysis of the ohmic metallised samples, the detection limits of Au, Ge and Ni were about 1-5 x $10^{16}$ atoms/cm$^3$. For these samples, standard SIMS profiling introduced artifacts due to limits in depth resolution. The sputtering mechanism introduced roughening of the crater bottom, especially in poly-crystalline materials where material was removed preferentially along crystal orientation. This resulted in degradation of the depth resolution, which was crucial in estimation of the depth of diffusion. The interference from memory effects of the metal layers also masked the low concentrations of the actual diffusion. Hence, SIMS profiling from the backside of the sample was resorted to [7,8]. The substrate was polished to about 1μm and profiled through the thin substrate side into the region of diffusion. The

profiles acquired from backside SIMS indicated a sharp drop from maximum concentrations in the contact layers to the much lower background levels in the semiconductor.

### 2.5.5. Transmission Electron Microscopy

In a transmission electron microscope (TEM), a focused electron beam with energy of about 100 - 300keV is incident on a thin sample. Signal in TEM is obtained from both deflected and undeflected electrons that penetrate the sample thickness. Signal is delivered to a detector with the help of a series of magnetic lenses at and below the sample position. The detector is a fluorescent screen or a film plate. The spatial information in the signal is magnified by 50 times to as high as $10^6$. Magnification range of this order is possible due to the small wavelength of incident electrons. TEM has high lateral spatial resolution as it uses a highly focused electron beam as a probe.

TEM offers two methods of specimen observation, diffraction mode and image mode. In the diffraction mode, a spot pattern is produced on the screen from a single crystal; a powder or ring pattern from a polycrystal; and a series of diffuse halos from a glassy or amorphous material [6] Diffraction information such as the crystal group can be obtained from very small areas of the sample. The image can contain contrast due to other aspects – mass contrast, due to spatial separations between distinct atomic constituents; diffraction contrast, in the case of crystalline defects resulting from scattering of the incident electron wave by structural defects; and phase contrast.

**Fig. 2.8. Technai 20T Analytical TEM**

During this work, cross-section TEM (XTEM) was performed using Technai 20T analytical TEM (FEI, The Netherlands). Energy dispersive x-ray spectroscopy (EDS) system (SUTW detector, EDAX, USA) attached to the TEM was employed for phase analysis. The specimens were prepared to electron transparency and investigated using a low-background double-tilt holder for chemical composition studies. A CCD system attached to the microscope was used to acquire the images

and view them on an LCD monitor. The transmitted beam through the specimens provided information of the microstructure with high resolution of about 0.2nm.

### 2.5.6. Scanning Electron Microscopy

Scanning electron microscopy (SEM) provides a highly magnified image of the surface of a material. Topographical and compositional information near surface regions with a resolution of few nm and magnifications of about 10X – 300,000X are possible. In the SEM, a source of electrons is focused (in vacuum) into a fine probe that is rastered over the surface of the specimen. As the electrons penetrate the surface, a number of interactions occur that can result in the emission of electrons or photons from (or through) the surface. A reasonable fraction of the electrons emitted are collected by appropriate detectors, and the output is used to modulate the brightness of the cathode rays tube (CRT), thereby producing an image. When a high-energy primary electron interacts with an atom, it undergoes either inelastic scattering with atomic electrons or elastic scattering with the atomic nucleus. In an inelastic collision with an electron, some amount of energy is transferred to the other electron. When the energy of the emitted electron is less than about 50eV, by convention it is referred to as a *secondary electron* (SE), or a *secondary. Backscattered electrons* (BSEs) are considered to be the electrons that exit the specimen with energy greater than 50eV, including Auger electrons.

SEM was carried out using a Leo 440i SEM system. The system was operated at 15-20kV. Topological information from the alloyed samples was gathered in the secondary electron mode. EDS (Oxford) facility fitted to the system was used for elemental analysis.

For the SEM study of the etched area under ohmic contacts, the contact metallisation was etched using the standard gold etchant $KI/I_2/H_2O$::4g:1g:40ml [5].

### 2.5.7. Atomic Force Microscopy

Atomic Force Microscopy (AFM) is a real-space imaging technique that produces topographic images of a surface with atomic resolution in all three dimensions. AFM uses a sharp tip mounted on a flexible low-stress $Si_3N_4$ cantilever with an integrated, square pyramidal tip. When the tip comes within a few Å of the surface of the sample, repulsive van der Waals forces between the atoms on the tip

and those on the sample cause the cantilever to deflect [6]. A piezoelectric transducer is employed to scan the tip across the sample. The image is generated by monitoring the position of the scanner in three dimensions. Vertical deflection is often monitored by beam-bounce detection system. Light from a laser diode is reflected from the metallised back of the cantilever into a position-sensitive photodiode. A deflection will then correspond to a specific position of the beam on the position-sensitive photodiode. The pressure exerted on the sample surface is small because of the force constant of the cantilever (typically 0.2N/m), and the high sensitivity of the position-sensitive photodiode to cantilever deflection.

Three imaging modes can be used to produce topographic images of sample surfaces, viz., contact mode, non-contact mode, and intermittent contact or tapping mode. During this study, AFM in the dynamic force mode (DFM) using SPA 400 of Seiko Instruments, Inc (figure 2.9) was used in the tapping mode Tapping mode is more applicable for soft samples, as the resolution is similar to contact mode while the forces applied to the sample are lower and less damaging. In this mode, the cantilever oscillates close to its first bending mode resonance frequency. However, the oscillation amplitude of the probe tip is in the range of 20 nm to 200 nm, and the tip makes contact with the sample for a short duration in each oscillation cycle. As the tip approaches the sample, the tip-sample interactions alter the amplitude, resonance frequency, and phase angle of the oscillating cantilever. In this thesis, the surface morphology of the ohmic metallisation samples was studied The frequency used for tip vibration was about 117-118KHz (tapping mode).


**Figure 2.9. SPA 400 atomic force microscope**

### 2.5.8. Thermal Imaging

For the purpose of thermal imaging of the ohmic contacts, the PCMs containing TLM structures were diced from the wafers and die-attached using the conventional AuSn eutectic on gold-plated


**Figure 2.10. Thermal imaging setup**

Cu-W carriers. They were wire bonded with 1-mil gold wire by thermosonic wedge bonding. Imaging was done using a non-contact thermal imaging camera, Compix 6000, Model PC2000/e. Magnification lens PC2100 was fixed on the IR camera, and the chips were focused by adjusting the field of view of the IR camera. The test set up is shown in figure 2.10. Voltage bias was then applied to the assembled structures and sufficient time was allowed for the attainment of stability of temperature. The emission from the top surface of the structures was scanned by the camera and analysed by suitable (WINTES) software to provide the temperature maps of all the zones. Measurement was conducted at 24±1°C. The emissivity of chip surface was assumed to be 0.80. The thermal imaging studies were carried out SAMEER, Centre for Electromagnetics, Chennai, India [9].

### 2.5.9. Accelerated thermal aging

The objective of the elevated thermal aging tests was to establish reliability, both qualitatively and quantitatively. About 12 packaged TLM structures each were chosen for the tests at three different chamber temperatures, viz., 185°C, 200°C and 230°C. Prior to subjecting the devices for the tests, they were verified for any defects due to assembly by performing the following tests.

(i) Constant acceleration tests at 15000g

(ii) Temperature cycling: 10 cycles at +150°C and -60°C, with a dwell time of 30 min each

These tests were necessary to ensure that the packaged TLM structures do not fail early and not influence the accelerated thermal aging tests.

The packaged TLM structures were subjected to the life tests in burn-in chambers (figure 2.11). The inset picture shows the devices inside a chamber. The mandatory minimum duration to carry out life tests is 2000hrs. However, tests on the packaged TLM structures were continued till 4000hrs in order to obtain failures with certainty. A total of

**Figure 2.11. Burn-in chambers used for life tests. The inset picture shows the packaged devices.**

12,000 to 16,000 hours of chamber time were logged. However, during the course of these accelerated tests, the tests were interrupted at regular intervals and the packages were taken out for $R_c$ measurements. All measurements were carried out within 48 hrs of the removal from the chamber. The drift in the values of $R_c$ was estimated after each measurement.

This test was also useful in understanding and estimating the thermal stability of ohmic contacts.

### 2.6. Specimen preparation techniques for XTEM

Special techniques were used to prepare specimens for XTEM characterization. These techniques, developed at Defence Metallurgical Research Laboratory (DMRL), Hyderabad, were adapted for the samples with ohmic metallisation [10].

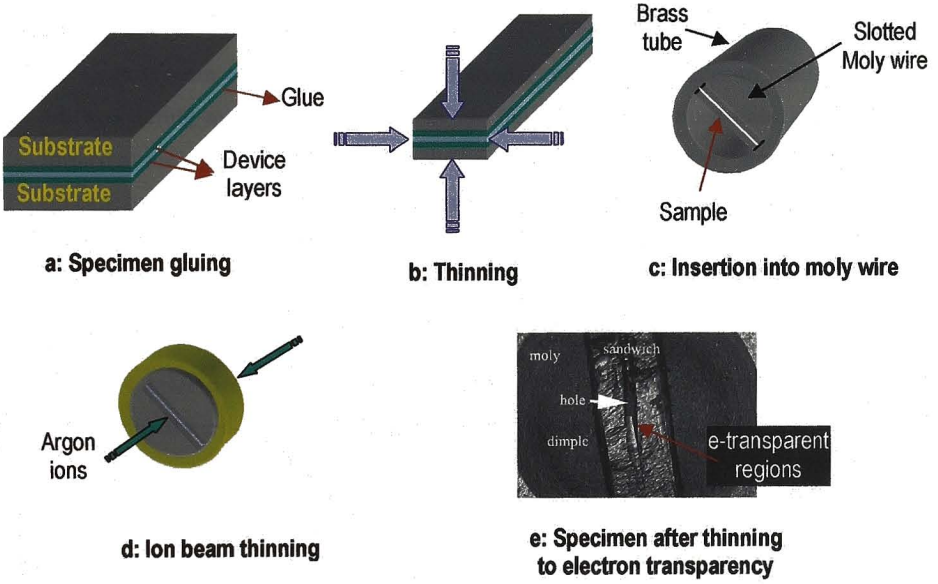


**Figure 2.12. Schematic showing different steps in the preparation of specimens for XTEM.**

Figure 2.12 illustrates the technique for the preparation of samples for cross-sectional TEM (XTEM). As shown in figure 2.12a, two pieces of the sample, cut into rectangular strips of about 10 mm length and 2.5 mm width, were sandwiched

together with a fast-curing epoxy. For example, the top device layers of MESFETs, i.e., the $n^+$-GaAs contact layers of both the pieces were facing each other. The substrate sides of the sandwich structure were then lapped on both sides to reduce the total thickness to about 0.3 mm (figure 2.12b). The sandwich was then inserted in a slotted (slot width ~ 0.3 mm and slot length ~ 10 mm) molybdenum rod (2.5 mm diameter) and bonded with the help of epoxy. The molybdenum rod-sandwich assembly was inserted into a brass tube (length: 15mm, inner diameter: 2.5 mm, and outer diameter: 3 mm) and again bonded with epoxy (figure 2.12c). It was ensured that the outside diameter of the molybdenum rod matched closely with the inner diameter of the brass tube so that the sample-molybdenum assembly was held firmly by the brass tube. After curing of the epoxy, discs with a thickness of ~ 200 μm were cut (figure 2.12d) using a low-speed diamond saw (Isomet, Model 11-1180, Buehler, USA). The discs were thinned and polished to a thickness of about 125 μm. They were then argon ion-milled to achieve electron transparency (figure 2.12d). The ion milling was carried out on a Duomill (Model 600, Gatan, USA). During ion milling, the samples were cooled using a liquid nitrogen cold stage in order to minimize the artifacts during milling. The process of ion milling was continued until a hole was formed at the center of the disc, with the edges of the hole being electron-transparent (thickness of the electron-transparent region is usually between 75 and 150 nm) (figure 2.12e).

## 2.7. Conclusion

A brief description of all the important experimental and characterization facilities used during the thesis work has been presented along with the conditions and specifications.

## 2.8. References


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# Chapter III

## Ohmic contacts to MESFETs

*Process parameters of alloying temperature and time were studied for obtaining very low contact resistances. Contacts were characterized by backside SIMS, TEM, thermal imaging, and electrical parameters of devices and MMICs. Also, the contact surface morphology was examined using AFM and SEM to correlate roughness with contact resistance. The results are presented and discussed*

### 3.1. Introduction

Alloying experiments were done between 380°C-420°C, at a fixed time of 150 seconds. The next set of experiments was performed to further optimize the alloying time at temperatures of 390°C and 400°C, in order to select the best alloying temperature and time cycle for achieving the lowest contact resistance ($R_c$). To understand the effect of different alloying durations on the electrical parameters at higher temperatures above 400°C, experiments for different alloying times were also performed at 410°C and 420°C.

### 3.2. Results and discussion

#### 3.2.1. Contact resistance

The average contact resistances obtained for alloying experiments at different temperatures for 150 sec are shown in figure 3.1. Figure 3.2 shows the contact resistances for alloying at 390°C and 400°C for different alloying times. The lowest value of contact resistance of 0.04Ω-mm was obtained for 150 sec at 400°C. The typical contact resistances were about 0.05 Ω-mm.

Contacts formed at temperatures lower than 400°C, and at 400°C for lesser duration than 150 sec are designated as '*under-alloy*' contacts. Contacts alloyed at temperatures higher than 400°C, and at 400°C for durations more than 150 sec are termed as '*over-alloy*' contacts. Contacts alloyed at 400°C for 150 sec are called as '*optimally alloyed*' contacts.

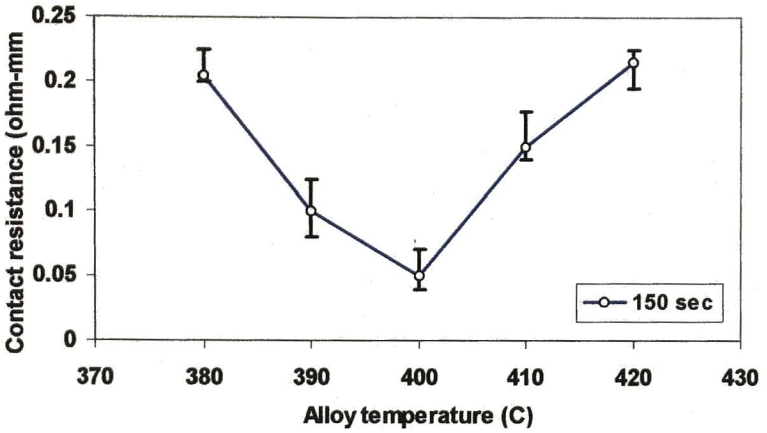



Figure 3.1. Average contact resistance at different alloying temperatures

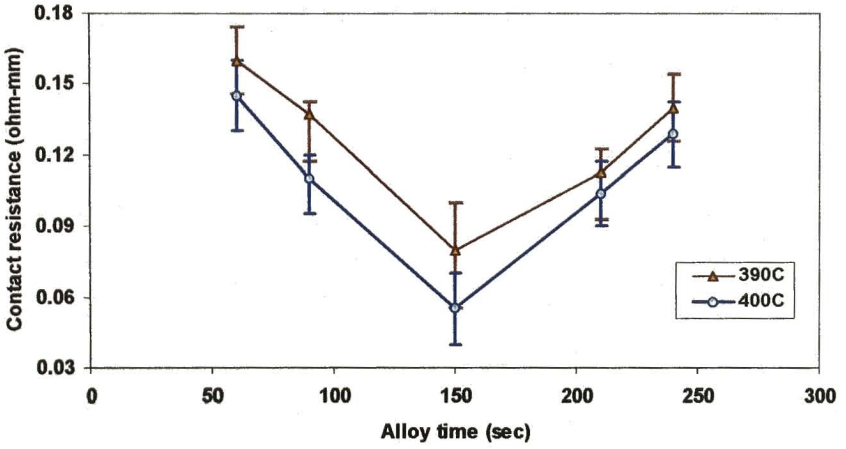



Figure 3.2. Contact resistances for alloying at 390°C and 400°C for different durations.

Contact resistance has been measured at two stages during fabrication of MMICs. Firstly, it is measured immediately after alloying, and secondly, after completion of all the fabrication steps, including the backside processing. The $R_c$ measurement just after alloying is referred to as '*initial level*', and the $R_c$ after complete wafer processing is called as '*final level*'. During MMIC fabrication, the wafer encounters various temperature cycles. For example, the lithography processes involve dehydration and other baking cycles; the nitride deposition processes involve heating cycles of about 250°C each time; the polyimide layer undergoes a curing step of about 330 to 350°C. Some of these thermal cycles independently or in a cumulative manner increase the contact resistance after the initial alloy formation stage. Throughout the entire processing of wafers, $R_c$ values of the wafers alloyed at 400°C /150sec cycle remained the lowest and exhibited stability. Figure 3.3a shows the distribution of initial $R_c$ values of the 'under-alloy' conditions and is compared with the values of optimally alloyed contacts in figure 3.3b. The $R_c$ values of the 'under-alloyed' contacts increased from an initial range of 0.12–0.16 Ω-mm to 0.4–0.7 Ω-mm at the final level (figure 3.4). Whereas, the initial range of the optimum alloyed contacts was 0.05–0.07 Ω-mm and increased only to a maximum of about 0.2 Ω-mm at the final level. The values of the optimal alloyed contacts were consistent and repeatable over a large number of batches of wafers.

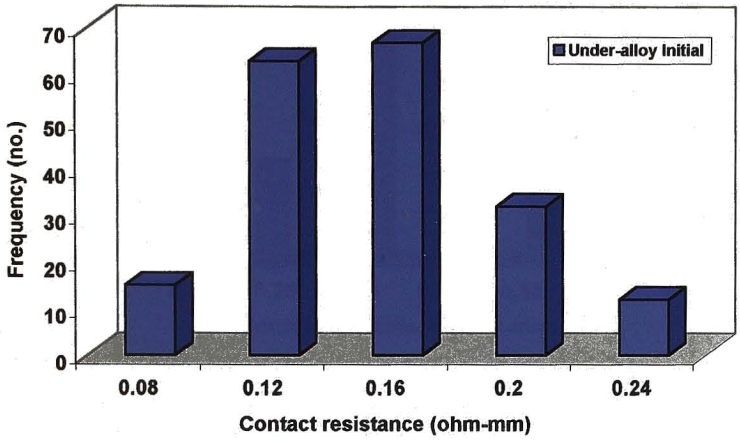
The morphology of the contacts was also studied during the optimization experiments. Contacts were observed under optical microscope for visible changes in morphology. The surface of the contact metal for alloying upto 400°C had a slightly granular appearance. At temperatures above 400°C, the metal surfaces became exceedingly granular, and the size of the features increased with temperature.

### 3.2.2. Characterization

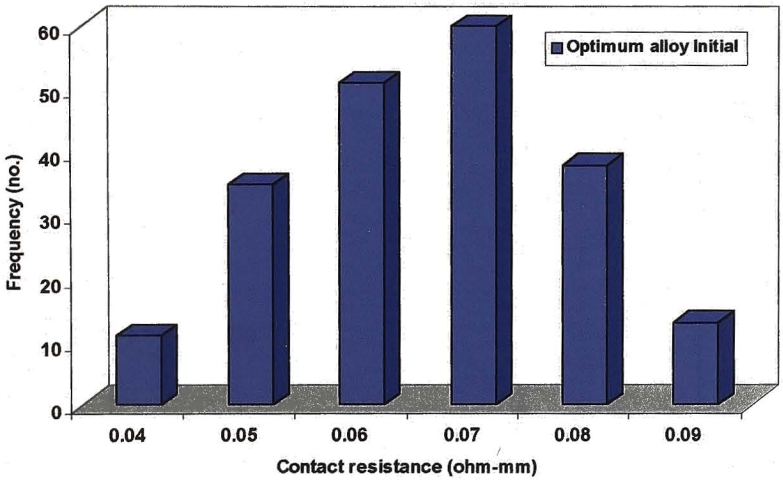
#### 3.2.2.1. Backside SIMS studies

The as-deposited sample was initially SIMS-profiled to serve as a reference. Figure 3.5 shows the abruptness and sharpness of the metal-semiconductor interface indicating the absence of any interdiffusion of the constituents of metallisation.

Figures 3.6 show the SIMS depth profiles of a sample alloyed at 390°C. The Ge profile shows a diffusion depth of about 800Å. A sharp roll-off from 2 x $10^{20}/cm^3$ at the interface to values below $10^{16}/cm^3$ within the $n^+$-GaAs region was noticed. Ni and




(a)




(b)

**Figure 3.3. Distribution of contact resistance immediately after alloying (initial) (a) for 'under-alloyed' contacts and (b) for optimally alloyed contacts.**

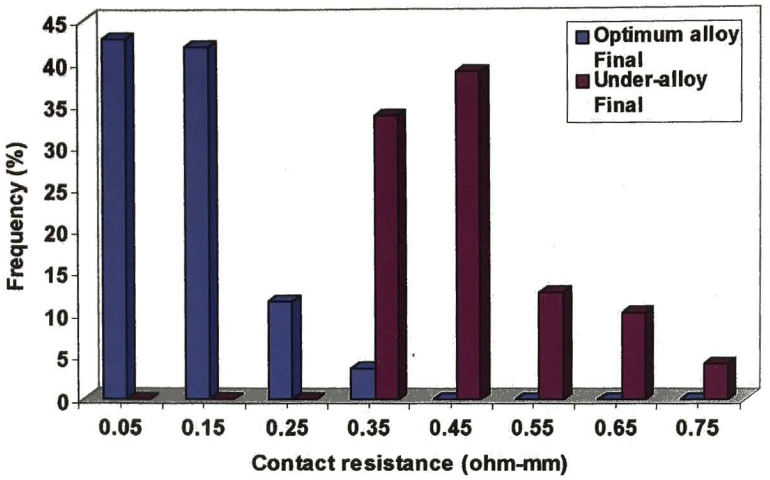



**Figure 3.4. Distribution of final contact resistance for optimally alloyed and 'under-alloyed' contacts.**

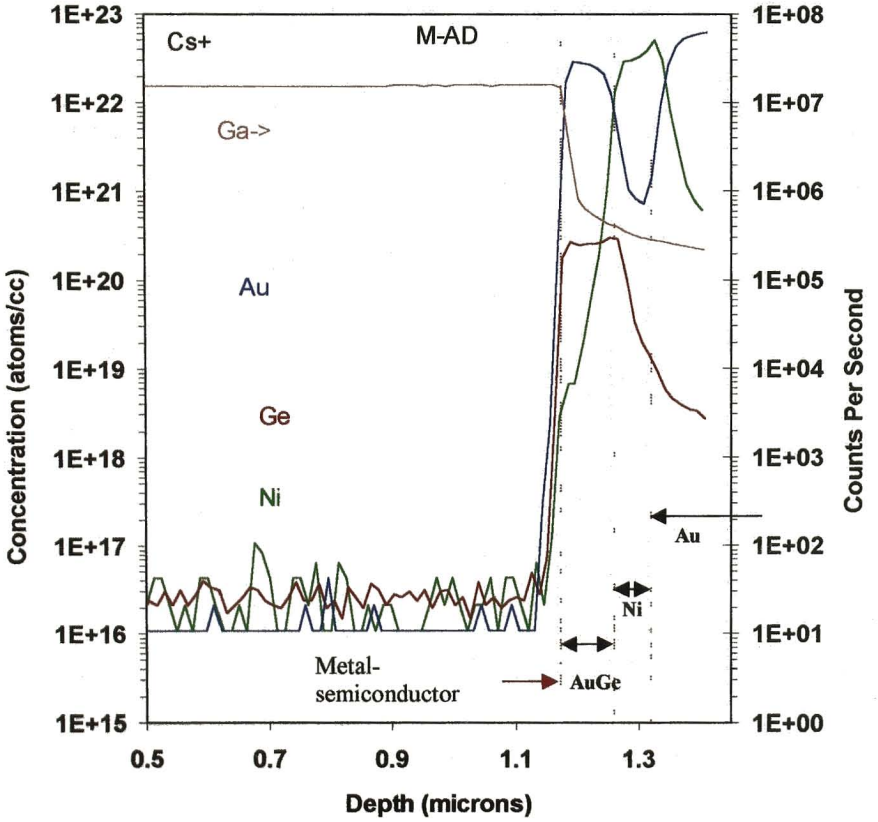



**Figure 3.5. Backside SIMS profiles of the as-deposited sample showing the abrupt and sharp metal-semiconductor interface, indicating the absence of any interdiffusion.**

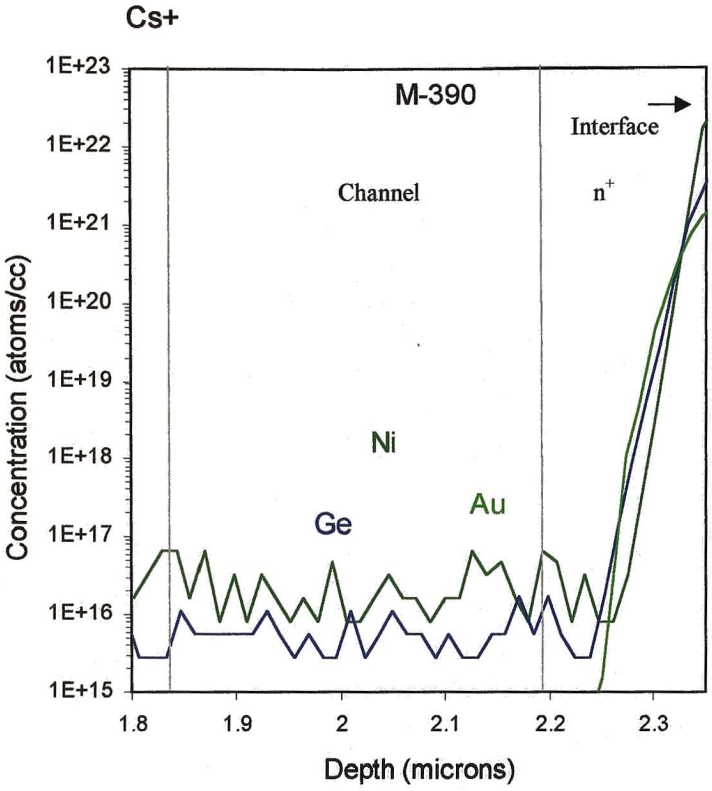



**Figure 3.6. SIMS profiles of sample alloyed at 390°C.**

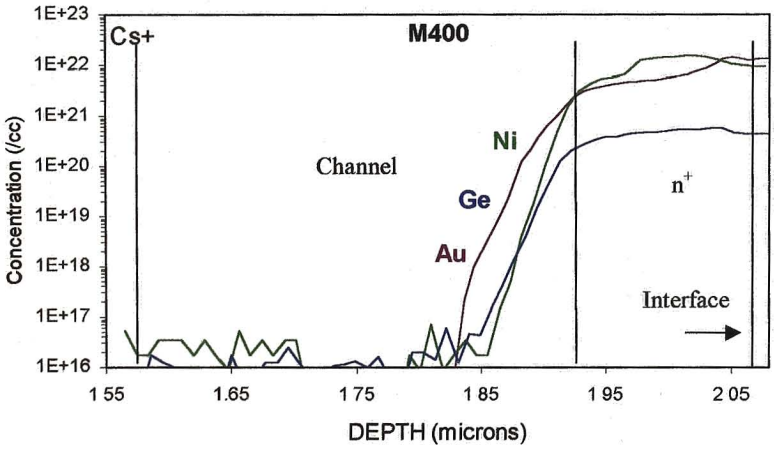



**Figure 3.7. SIMS profiles of sample alloyed at 400°C.**

Au concentrations followed the Ge profile in this sample. The elements are practically absent in the channel.

The SIMS profiles of optimally alloyed sample at 400°C are shown in figure 3.7. Maximum concentration of Ge was observed for this alloy cycle. The $n^+$ region has a maximum concentration of about 5.66 x $10^{20}/cm^3$, and remains nearly uniform in the $10^{20}/cm^3$ range. Further, a high concentration of about 2.05 x $10^{20}/cm^3$ is also observed at the $n^+$ contact-channel layer interface for this alloy recipe The diffusion depths are about 2400 Å for alloying at 400°C. The Au and Ni profile tail the Ge profile, but with a higher concentration of about 7 x $10^{21}/cm^3$ and 1 x $10^{22}/cm^3$, respectively.

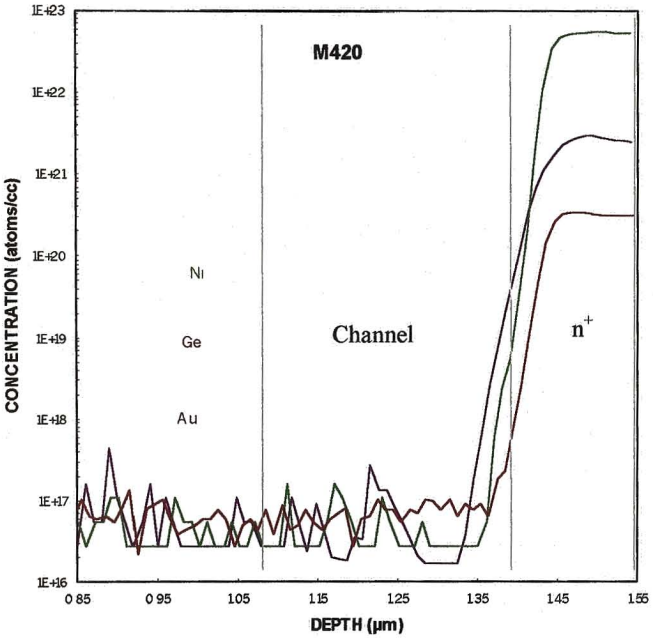



**Figure 3.8. SIMS profiles of sample alloyed at 420°C.**

Figure 3 8 shows the SIMS profile of a sample alloyed at 420°C The sample had a Ge concentration of 3 x $10^{20}/cm^3$ within the $n^+$ layer. The Ge concentration at the $n^+$-n interface is about $10^{17}/cm^3$ in this sample. While the Ni concentration was higher in the $10^{22}/cm^3$ range, the Au profile was lower in the $10^{21}/cm^3$ compared to the optimally alloyed sample.

The major observations from SIMS are as follows:

(1) The Ge concentration within the diffused regions in the optimally alloyed sample is very high.

(2) A penetration of Ge upto about 1000 Å inside the channel is observed in the optimally alloyed sample. The 'tail' region of Ge diffusion profile has very high concentration, and coincides with the peak of the implanted Si concentration of the channel.

### 3.2.2.2 Cross-section TEM studies

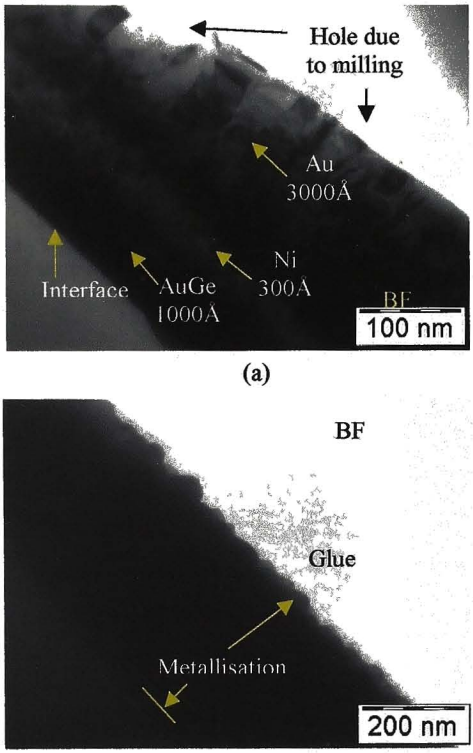



**Figure 3.9. (a) The Au overlayer of the as-deposited sample with small-sized grains. The thicknesses of metal layers are shown (b) Surface roughness of the metallisation.**

The as-deposited metallisation sample was used as a reference. The bright field (BF) TEM image of the as-deposited ohmic metal (figure 3.9a) shows the

individual metallisation layers of AuGe, Ni and Au, and a sharp metal-semiconductor interface. The overlayer of Au consists of small-sized grains, which were closely packed. Their size and shape were random, and mostly resembled the columnar type. The BF image of a section of the surface of the sample, shown in figure 3.9b, reveals the typical surface roughness.

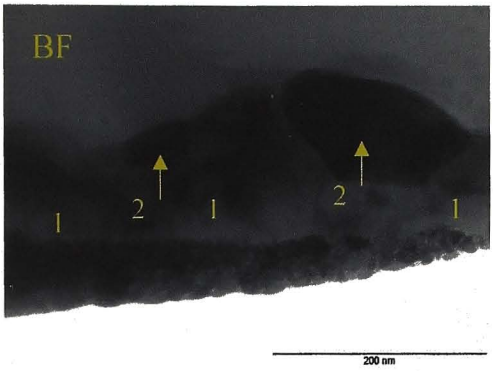
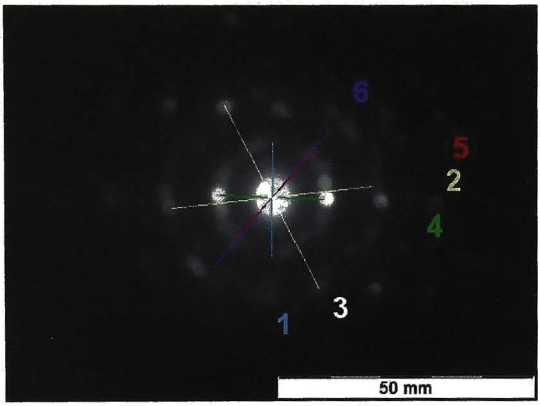



**Figure 3.10. Diffusion layer observed for the sample alloyed at 390°C showing two different grains, viz., (1) Ni-rich and (2) Au-rich.**




| № | $d_{expt}$ (Å) | $d_{theoretical}$ (Å) |
|---|---|---|
| 1 | 1.628 | 1.621 |
| 2 | 1 007 | 1 005 |
| 3 | 0.999 | 0.99 |
| 4 | 1.930 | 1 938 |
| 5 | 1.760 | 1 760 |
| 6 | 1.174 | 1.170 |

**Figure 3.11. Diffraction pattern from a Ni- and As-rich grain and matches with the data of $Ni_3Ge_2As_6$.**

A sample alloyed at 390°C showed diffusion of the ohmic metal. The BF image in Figure 3.10 shows the diffusion layer containing two types of grains, identified as '1' and '2' in the figure. The EDS spectra showed that grain '1' was Ni-

rich, and '2', was Au-rich. The microdiffraction pattern from the Ni-rich region was indexed, as shown in figure 3.11, and the indexed 'd' spacings matched nearest to the compound of $Ni_3Ge_2As_6$. The alloy diffusion was dominated by the Au-rich phase. The Au overlayer, shown in BF image figure 3.12, is seen with more developed columnar grains, larger compared to the as-deposited sample. Surface roughness was observed in this sample, but less compared to the as-deposited sample.

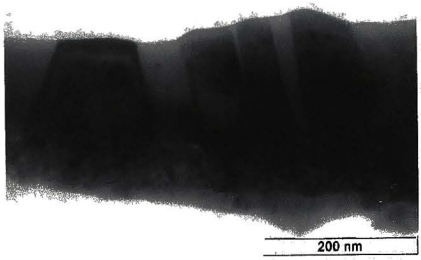



**Figure 3.12. BF image of 390°C sample showing columnar Au grains.**

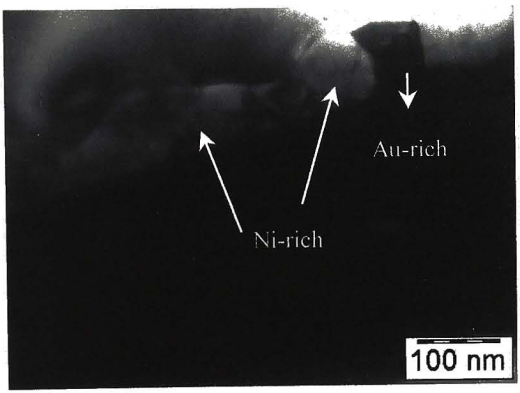
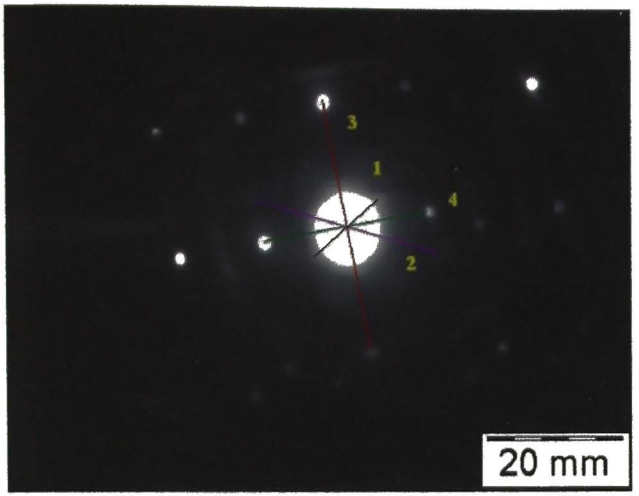



**Figure 3.13. Diffusion grains in the sample alloyed at 400°C showing two different grains. The Ni-rich grain is found dominant.**

Figure 3.13 is a dark field (DF) image of the diffusion grains formed within the sample alloyed at 400°C. Two different types of grains were observed, one rich in Ni, and another rich in Au. Grains of the former type were present more in the

diffusion region, as seen in the TEM images. The diffraction pattern from the Ni-rich grain was indexed (figure 3.14) and values of the 'd' spacings matched with the data of the $Ni_3Ge_2As_6$ compound. The Au overlayer had larger elongated Au-rich grains (figure 3.15). The top metallisation was also noticed to be very smooth.




| № | $d_{expt}$ (Å) | $d_{theoretical}$ (Å) |
|---|---|---|
| 1 | 2 616 | 2.612 |
| 2 | 1.216 | 1.220 |
| 3 | 0.895 | 0 990 |
| 4 | 1.375 | 1.377 |

**Figure 3.14. Diffraction pattern from a Ni-rich grain of the sample alloyed at 400°C.**

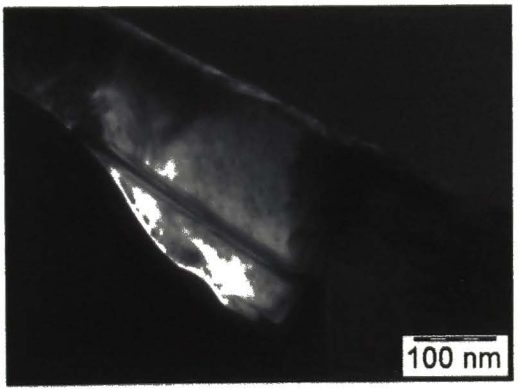



**Figure 3.15. The top surface of the metallisation showing less roughness, and also larger Au-rich grains**

Figure 3.16 shows the diffusion and formation of Au-rich and Ni-rich grains in a sample alloyed at 420°C. Au-rich grains were noticed to be dominating in the

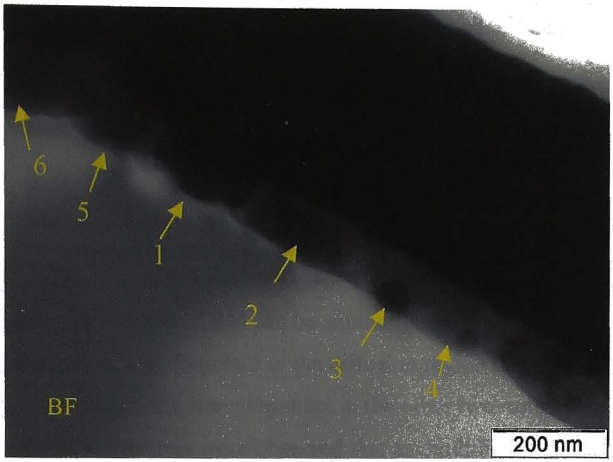



**Figure 3.16. Presence of Au-rich and Ni-rich grains in the 420°C sample.**

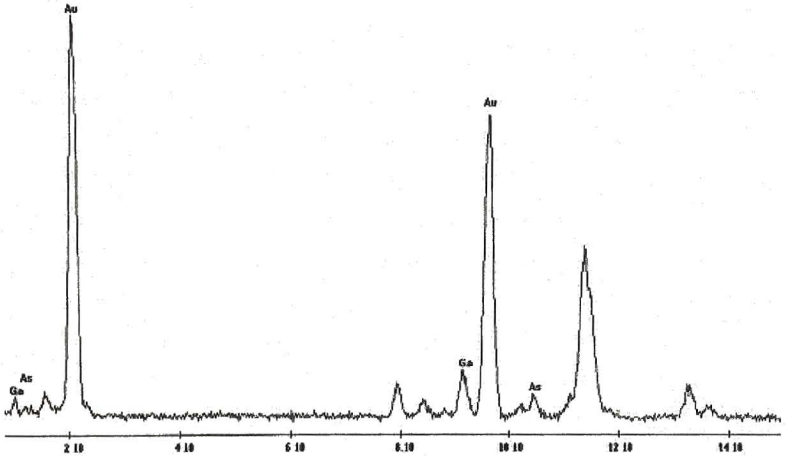



**Figure 3.17. EDS profile from the Au overlayer.**

diffusion area. The grains identified in the figure as '2', '4' and '5' were Ni-type, whereas, the remaining were Au-rich. Large 'blisters' or protrusions on the surface of the metallisation were observed due to outdiffusion of Ga and As, as seen from the

EDS spectrum figure 3.17. The Au overlayer is seen with larger Au-rich grains, as shown in the DF TEM image of figure 3.18.

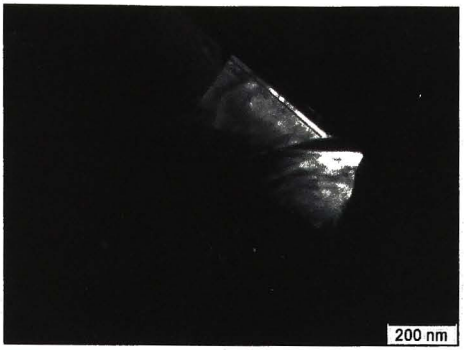



**Figure 3.18. DF image of large Au-rich grains of sample alloyed at 420°C.**

The major observations from TEM can be summarised as follows.

1. The Ni-rich phase was dominant in the diffusion region of 400°C sample.
2. The Au-rich compounds were dominant in the other two samples.
3. Large surface protrusions were observed due to outdiffusion of Ga and As in the 420°C sample.
4. The size of the Au-rich grains in the overlayer increased with alloying temperature.

Formation of highly conducting $n^+$-layers at the interface, due to doping of Ge, has been known as the mechanism of low resistance contact formation [1, 2]. Above the melting point of the eutectic, the liquid state of the AuGe alloy aids rapid in-diffusion of germanium. Here, nickel plays the role of a catalyzer and a wetting agent, and forms compounds with As. The function of indiffusion of Au is as important as that of Ni. The profile of Au is found to be following the Ge profile, in the same way as Ni. This forms gold-rich compounds such as AuGa within the semiconductor, as observed in XTEM experiments above [3, 4]. Formation of AuGa during alloying as a result of continuous inward penetration of Au leads to substantial creation of gallium vacancies ($V_{Ga}$) in the diffused regions. Presence of these vacancies along the depth seems to be the main requirement for Ge in-diffusion and doping. Ge atom located at one $V_{Ga}$ in the host lattice, diffuses by dislocating itself with thermal energy (during alloying cycle), and moves interstitially before being trapped by another $V_{Ga}$ [5]. In the optimum alloy sample, the SIMS concentration profile of Ni followed the Ge profile closely. Diffusion coefficient, D, was estimated from the fundamental solution

to diffusion equation given by Fick's second law [6]. Figure 3.19 shows the graph of logarithmic D versus $10^3/T$ and the diffusion constant, $D_0$, was obtained to be 2.1 x $10^{-10}$ $cm^2/sec$. The lower values of diffusion constant suggest the above mechanism of doping. This mechanism is known to primarily depend on the availability of vacancies. Thus the most critical condition to be satisfied is the inward diffusion of Au for sufficient Ge doping of GaAs.

The dominance of the Ni-rich compounds in the diffusion region of the 400°C sample is supported by the higher Ge concentration observed by SIMS in the same sample. In the 'under-alloy' sample, Au-rich phase was dominant, in agreement with the observation from SIMS that the diffusion of Ge was still incomplete. In the sample alloyed at 420°C, Au-rich phase was dominant. Outdiffusion of Ga and As, and even Ge was observed in this sample. From these observations it can be understood that low contact resistances obtained for the optimally alloyed sample was due to high doping of Ge and the dominance of the Ni-rich compound in the diffusion region. While insufficient diffusion in the 'under-alloy' sample resulted in high contact resistances, the amphoteric behaviour of Ge became dominant in the 'over-alloyed' sample, leading to compensation and hence, higher contact resitances.

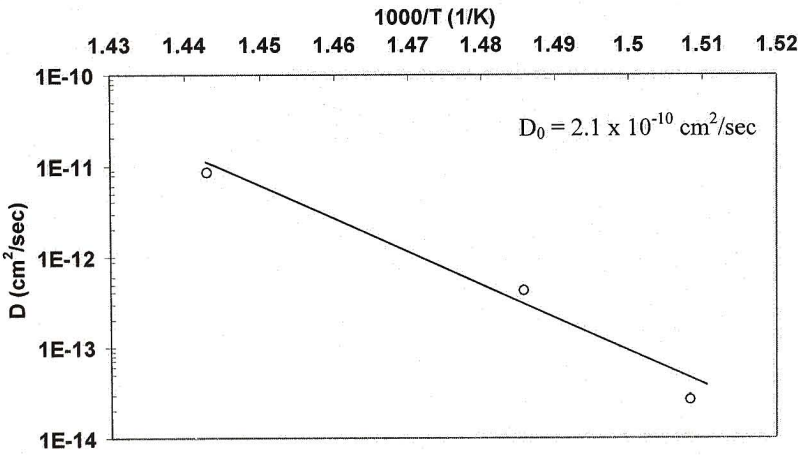



**Figure 3.19. Diffusion coefficient vs. $10^3/T$ of Ge**

### 3.2.3. Surface morphology studies

#### 3.2.3.1. SEM studies

SEM was used to understand the surface morphology of the contacts. The 'reacted' GaAs regions below the contact pads were also studied after removing the metal layers by wet etching.

The metallisation surfaces of the samples alloyed at 390°C and 400°C remained relatively featureless compared to that of 420°C. Between the 390°C and 400°C samples, the morphology of the 400°C looked more smoother. The 420°C sample had a larger spread of small-sized 'blisters' and few large-sized blisters, as can be seen in figure 3.20.

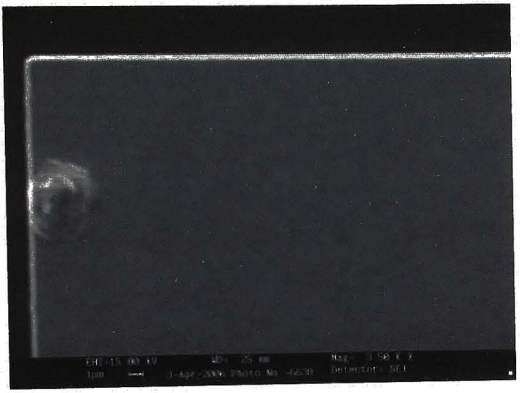


**Figure 3.20. A large 'blister' on the surface of the 420°C-alloyed sample seen alongside the smaller ones.**

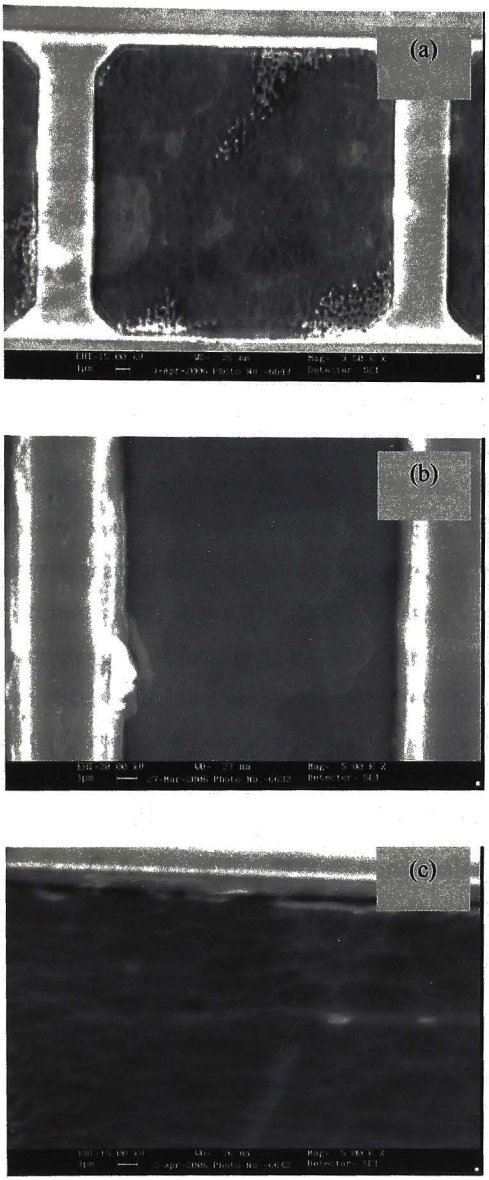



**Figure 3.21. Surfaces of the alloyed contacts after removal of the metallisation. (a) 390°C sample showing local variations and rough surface, (b) 400°C sample showing large and smoother features, and (c) 420°C sample with large variations of the surface features indicating higher roughness.**

The patterns on the samples after etching of the metallisation were examined and compared with each other. Figure 3.21(a) shows the 'reacted' GaAs surface of the wafer alloyed at 390°C. This had smaller features but higher local variations in roughness. In contrast, figure 3.21(b) shows the wafer alloyed at 400°C with larger features, and the local variations of roughness within such a feature was very minimal. Figure 3.21(c) shows the sample alloyed at 420°C having random variations of feature sizes indicating higher roughness. It appeared that the 'reacted' region acted as a kind of template for the surface morphology.

### 3.2.3.2. AFM studies

Surface roughness of all the samples was studied using AFM. Figure 3.22 shows the AFM images and line scans across the pads of the ohmic contacts of samples alloyed between 380°C and 420°C. A gradual smoothening of the surface with increasing temperature is noticeable from the line scans. However, the dominance of 'blisters' was noticed above 400°C. While the scan of sample alloyed below 400°C shows higher local variations of roughness, the sample alloyed above 400°C shows broad peaks and valleys. The RMS roughness values of the samples at these alloy temperatures are plotted in figure 3.23. The lowest RMS roughness of about 3.5 nm was obtained for the sample alloyed at 400°C. The increasing RMS roughness above 400°C was mainly due to the increasing size and density of 'blisters'. RMS roughness of the as-deposited metallisation was more than 7 nm.

During alloying above the eutectic temperature, AuGe alloy melts and dissolves a thin layer of GaAs. Interdiffusion of alloy materials from the metallisation, and the cations and anions from the substrate take place. While Au, Ge and Ni diffuses into the semiconductor and forms various compounds, gallium outdiffuses from the $n^+$-GaAs surface into the gold over-layer, resulting in the formation of AuGa compounds in the over-layer [7]. The surface morphology of low resistance contacts is reported to be rough [8]. It is reported that with increase in alloying temperature the contact resistance reduces, but at the same time surface roughness increases due to outdiffusion. On the other hand, we have shown that it is possible to obtain low resistance contacts with lower surface roughness. We have observed that the surface roughness due to Ga outdiffusion becomes dominant only beyond the optimum alloying temperatures of 400°C. This phenomenon is attributed to a competition

between grain smoothening due to coalescence, and grain coarsening due to outdiffusion.

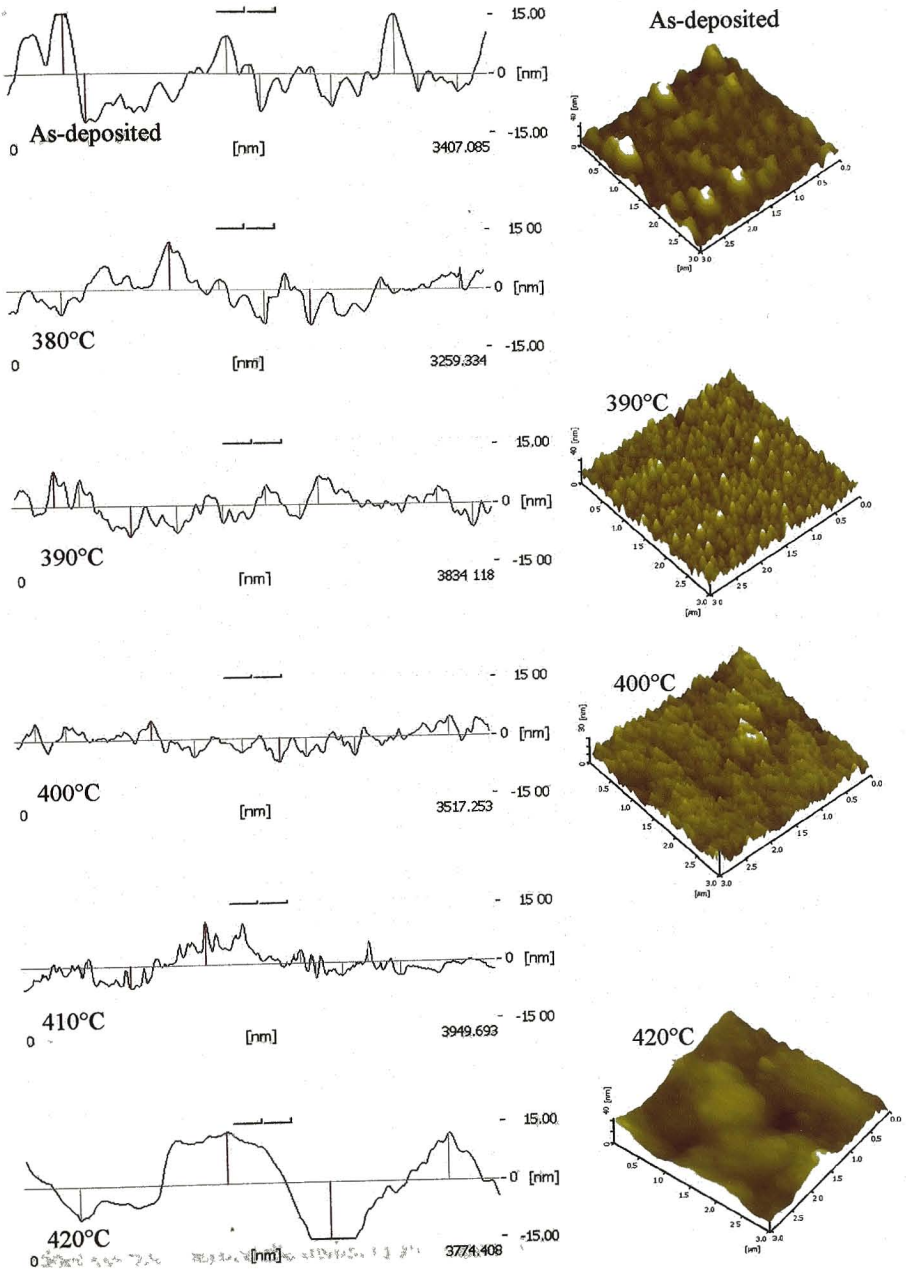



**Figure 3.22. AFM images and line scans indicating the roughness of the contact surfaces for different alloying temperatures.**

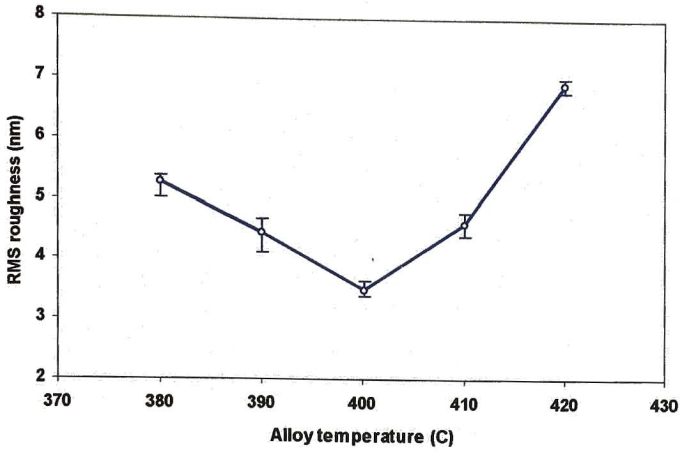



**Figure 3.23. RMS roughness of samples alloyed between 380°C and 420°C. Minimum roughness was obtained for alloying at 400°C.**

When the initial grain sizes of the metallisation are less than the film thickness, the metallisation can be assumed to consist of finer layers of thin films. These finer layers evolve due to coalescence of the smaller grains formed during evaporation. The driving force for coalescence is to maintain a minimum overall surface area of the grains. It is known that in metals such as Al, Ag, Au and Cu, the higher surface mobility of the adatoms leads to continued structure evolution [9]. Surface morphology alters due to the fact that grain growth continues to occur during the post-deposition heat treatments. After the onset of grain growth, the average size of the grains increases. The surface begins to smoothen due to formation of columnar grains, separated by grain boundaries [10]. Grains enlarge further with temperature leading to equiaxial grain formation, and the number of grains decreases eventually This activity ceases when the grain sizes become comparable to the film thickness. The evolution of the morphology of ohmic metallisation is interfered by the increasing outdiffusion from GaAs. The reduction of roughness of the as-deposited ohmic metallisation proceeds until optimum alloying conditions, and is overtaken by the outdiffusion process at higher temperatures. In fact, the process of smoothening does continue beyond the optimum alloy formation temperature, but it is the increase in outdiffusion that masks the effect, resulting in coarsening of the surface.

Figure 3.24 traces the evolution process of the surface morphology of ohmic contacts of MESFETs with respect to the ratio of $T_s/T_m$, where, $T_s$ is the post-deposition annealing (or alloying) temperature, and $T_m$ is the melting temperature of gold. The overlayer of Au in the as-deposited sample (figure 3.9a) was seen with closely packed small-sized grains. Their size and shape were more random, but resemble the columnar type. Higher surface roughness of the as-deposited metallisation was noticeable during XTEM and AFM characterization. In the 'under-alloyed' sample, the Au overlayer is seen with more developed columnar grains (figure 3.12). At 400°C, the roughness is very less compared to the as-deposited and

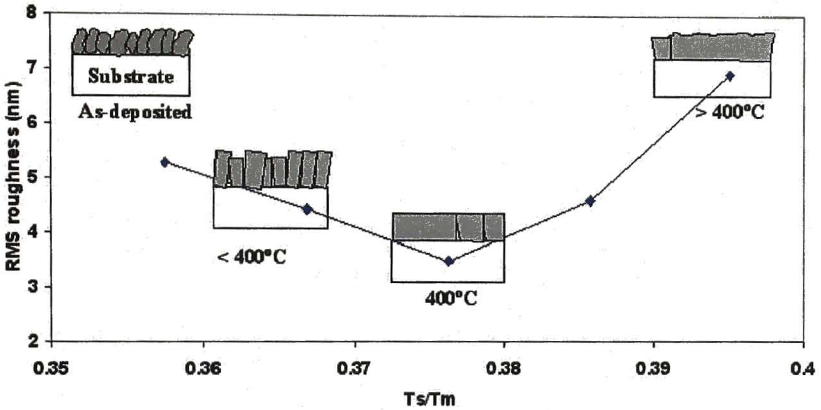



**Figure 3.24. Evolution of surface morphology of ohmic contacts of MESFETs with respect to the ratio of $T_s/T_m$. The transition from surface smoothening to surface roughening occurs near 0.375 $T_m$.**

the 'under-alloy' conditions. Here, the Au-rich grains were seen to be large-sized (figure 3.15). The transition from surface smoothening to surface roughening occurs near $0.375T_m$. Above this temperature, the Au overlayer is seen with larger Au-rich grains and 'blisters' due to strong outdiffusion. Contact metallisation worsens beyond $0.40T_m$, and electrical measurements become impracticable at about $0.41T_m$ [11].

It was observed that the integrity of the surface morphology leads to better contacts. It was shown that the roughness of the contact surface was found to follow the trend of contact resistance. Low values of roughness indicate that the process

window is large for the optimum alloy cycle, and hence ensures stability of contact formation.

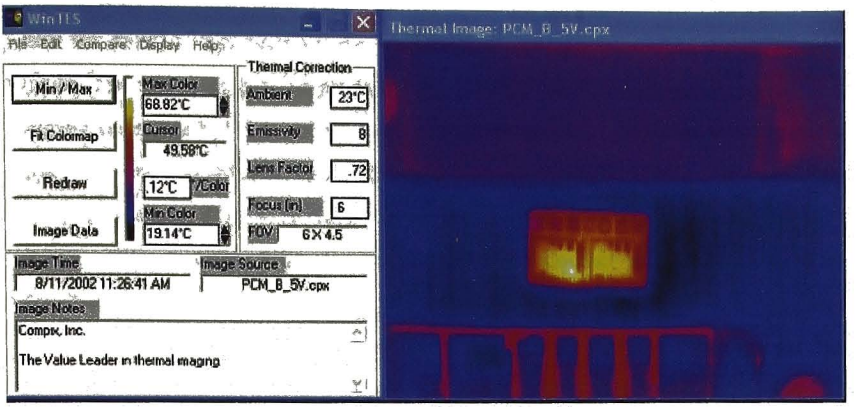
### 3.2.4. Electrical characterization

#### 3.2.4.1. Thermal imaging

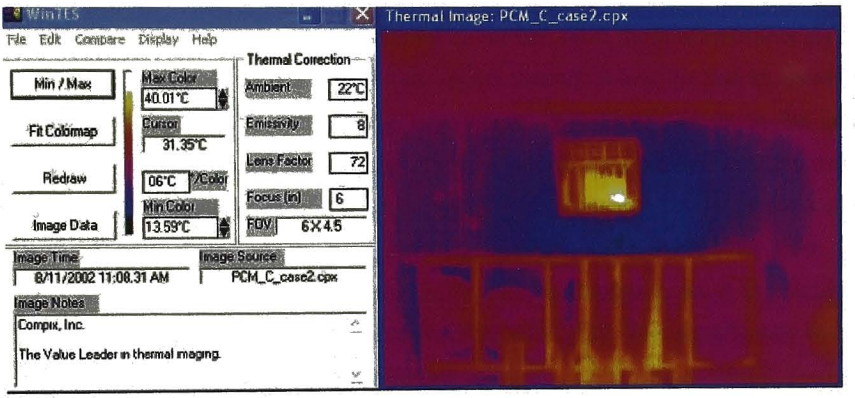
Representative TLM structures from the 'under-alloy' and optimal alloy were chosen for this study and assembled in individual packages. The 'final' $R_c$ values of PCM_B ('under-alloy' case) and PCM_C (optimal alloy case) were in the range of 0.5 – 0.6 Ω-mm and 0.06 – 0.08 Ω-mm, respectively.

Bias was applied across the pair of TLM pads separated by 12μm distance. When PCM_B was biased at 1V, a current of 29mA was measured. Once equilibrium was reached, the IR camera measured a temperature of 27.34°C. When PCM_B was biased at 5V, a current of 86mA was measured. The increase in temperature to 68.82°C is shown in figure 3.25a. The bias for PCM_C was set at the same current as that of PCM_B so that the heat generation for the actual voltage drop in both the cases could be compared. The device reached 86mA at 1.84V and the temperature of the hot zone was 40°C. The thermal image recorded during radiation is shown in figure 3.25b. The temperature measured for the two cases at 86mA show a difference of about 28°C between them. The surrounding package assembly region can be seen relatively colder compared to the hot zones of TLM.

The resistance across which power was being dissipated was lower for the optimally alloyed sample. The difference of 28°C between both the alloying conditions during bias was very high. Large heat generation in the 'under-alloy' case led to poor electrical and thermal performances.




(a)




(b)

**Figure 3.25. Thermal imaging of TLM at 86mA for (a) 'under-alloy' condition and (b) 400°C/150 sec. The hot zones are brighter compared to the adjacent package assembly.**

### 3.2.4.2. Access resistance

From the backside SIMS profiles, diffusion of germanium was observed only near the metal-$n^+$ interface for the 'under-alloy' cycle compared to the optimum alloy cycle. Therefore, in the 'under-alloy' conditions, the conduction of current will be mostly restricted to the $n^+$-contact layer, as illustrated in figure 3.26a. Whereas, in the optimally alloyed sample, penetration into the channel with high concentration levels, especially about 2.05 x $10^{20}/cm^3$ at the interface of $n^+$-n layers, is observed (figure 3.26b). This is responsible for reduction of the contact resistance. The inference acquired from the thermal imaging studies seems to be pointing in the same direction. The difference in peak surface temperatures (during thermal imaging) for 'under-alloy' and optimum alloy conditions for same values of current, reiterates that the resistance across which the power is being dissipated is lower for the optimal alloy case.

When the current path to the channel is traversed from the contact pad in the optimally alloyed device, one component of current, takes the low resistance path by using the volume of highly doped bulk region directly below the pad to access the channel. However, the conventional component, '$R_s$(lateral)', exists in the lateral direction between source and gate, along the $n^+$-GaAs region [12]. Since the contact area for the first component is more compared to the conventional lateral component, it is likely to have less current crowding leading to uniform carrier flow. This component '$R_s$(longitudinal)' (figure 3.27) will be dominant, as it is electrically parallel to the lateral component and lower in value [13]. This significantly reduces the overall resistance, and can be expressed as

$$R_s(effective) = R_s(lateral) \parallel R_s(longitudinal) \tag{3.3}$$

This modified the access region with the creation of a low resistance path for current flow. In the 'under-alloy' case, when current enters the channel, it would experience higher resistance at the interface of $n^+$-n layers and there would be higher dissipation in the form of Joule heating at this interface. Therefore, current across this interface would be thermionically emitted [14] and increases the contact resistance.

Thus, higher doping of $n^+$-layer is only a necessary condition, but not sufficient to obtain low contact resistances. Additional doping of the $n^+$-n interface and the channel region to about 1000Å is the sufficient condition to achieve low

contact resistances, as the resistance of this $n^+$-n interface plays a crucial role in minimizing dissipation of electrical energy during current conduction.

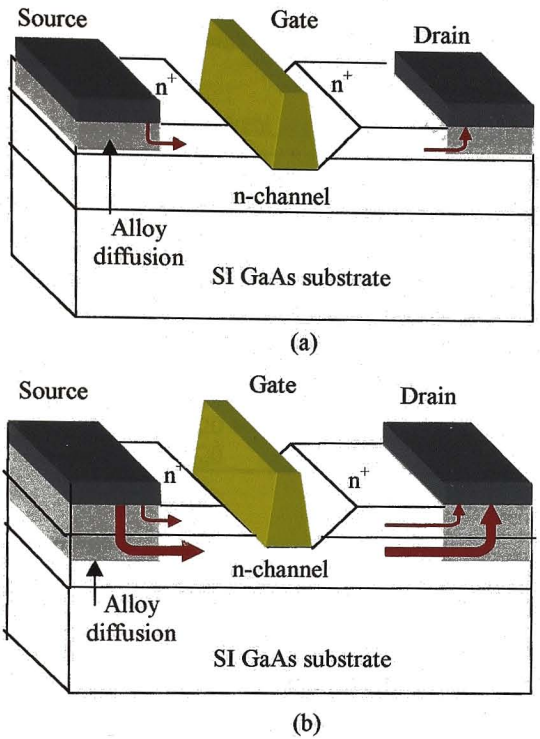



**Figure 3.26. Schematic of MESFET showing source-drain current flow in (a) 'under-alloy' case and (b) optimal alloy case. Current is restricted within the n⁺-GaAs in the earlier case.**

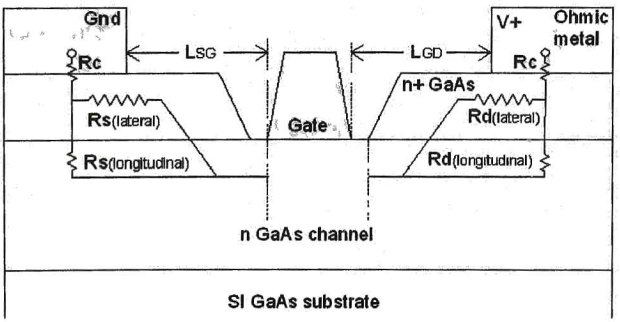



**Figure 3.27. Source-drain current flow through the low-resistance path represented by the longitudinal component of the access resistance in the optimal alloy case.**

### 3.2.4.3. Saturation voltage and current

The typical saturation current and voltage values obtained for different alloy temperature-time cycles are shown in table 3.1. $V_{sat}$ obtained for 'under-alloy' wafers were as high as 4.3V. Very high $I_{sat}$ values were obtained for devices alloyed at 400°C/150sec.

Table 3.1. Saturation current and voltage obtained for various alloy cycles

| S. No. | Temperature | Time | $I_{sat}$ (mA) | $V_{sat}$ (V) |
|---|---|---|---|---|
| 1 | 390 | 90 | 200 - 220 | > 3.8 |
| 2 | 390 | 150 | 200 - 220 | > 3.8 |
| 3 | 400 | 120 | 215 - 225 | 3.3 - 3.5 |
| 4 | 400 | 150 | 220 - 240 | 3.2 - 3.4 |
| 5 | 400 | 180 | 220 - 240 | 3.3 - 3.5 |
| 6 | 410 | 90 | 210 - 230 | > 3.6 |
| 7 | 410 | 150 | 210 - 220 | > 3.7 |
| 8 | 420 | 45 | 230 - 235 | > 3.6 |
| 9 | 420 | 150 | 210 - 215 | 3.6 - 3.8 |

### 3.2.4.4. Knee voltage

Knee voltages after gate fabrication have been particularly analyzed to study the effects of alloying. For the 'under-alloy' case, $V_{knee}$ values higher than 850mV were observed. For optimally alloyed wafers, lower values of about 650–700mV were obtained for the devices. The I-V characteristics of such MESFETs illustrating the above conditions are shown in figures 3.28. The low values obtained for optimal alloying signify the reduction in the resistance of the metal-semiconductor interface region.

### 3.2.4.5. Transconductance

The extrinsic DC transconductance ($g_m$) of the devices was measured after gate formation. Transconductance of the devices of gate width of 150μm (or a single gate) immediately after gate formation is called as '*initial* $g_m$'. Transconductance is measured only on single finger MESFETs until the formation of interconnects. After completion of front side fabrication of the wafer, the $g_m$ of standard MESFETs with four parallel gate fingers or the 600μm-gate width MESFETs is denoted as '*final* $g_m$'.

For the 'under-alloy' case, the peak values of initial $g_m$ were about 17-21mS (113-140mS/mm). About 19-23mS (126-153mS/mm) was obtained for the optimally alloyed wafers. The 'final' $g_m$ was in the range of 80-86mS (133-145mS/mm) for the

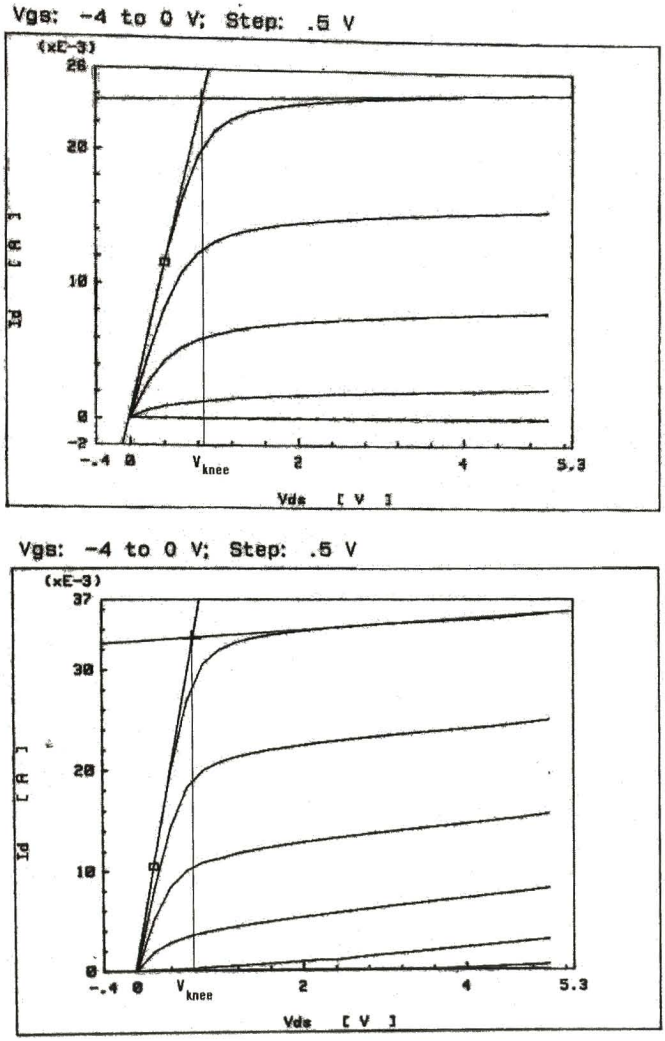



**Figure 3.28. $V_{knee}$ of 'under-alloyed' and optimally alloyed MESFETs shown in the I-V characteristics.**

wafers of optimal alloying, compared to 73-82mS (121-136mS/mm) for 'under-alloy' conditions. [The $g_m$ values do not linearly scale after interconnecting the four parallel

gates (i.e. 600μm FET). Hence, the $g_m$ per mm of the 600μm FETs are lower compared to that of the 150μm devices.]



### 3.2.4.6. R. F. parameters

For a 600μm MESFET, RF transconductance was between 85–100mS (141-167mS/mm) for the optimally alloyed wafers, as compared to 65–85mS (108-141mS/mm) for 'under-alloy' case.

The cut-off frequency ($f_t$), which is directly proportional to the $g_m$, increased from a range of 17.0-17.5GHz for the 'under-alloy' wafers, to 18.0-19.0GHz for the optimum alloyed wafers.

### 3.2.4.7. Effect on MMIC performance

We found that the microwave output power ($P_{out}$) of medium power amplifier (MPA) MMICs, designed to deliver 20dBm output power in X-band (8.0-12.0 GHz), was restricted to 18 - 19dBm over many wafers fabricated in batches. While investigating the cause, it was deduced that the low levels of power output was primarily due to very high ohmic contact resistances of the MESFETs. When the optimized contact alloying cycle was established and implemented, the desired power levels of 20 dBm were consistently obtained [13].

Figure 3.29 shows the schematic of the X-band MPA MMICs, which was a four-stage medium power amplifier with a gain of ~17 dB, and an expected $P_{out}$ of 20dBm (100 mW) (min) in the frequency range of 8.0 – 8.4 GHz. Different stages of this MMIC chain utilize MESFETs of different sizes for achieving the desired output power.

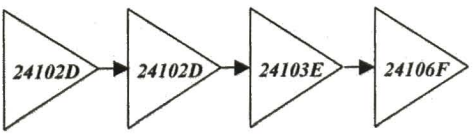





**Figure 3.29. X-Band Medium power amplifier assembly schematic showing the chain of MMICs**

A simplified estimate of the power output capability of a MESFET is given by

$$P_{out} = (I_m/8)(V_b - V_p - V_{knee}) \tag{3.13}$$

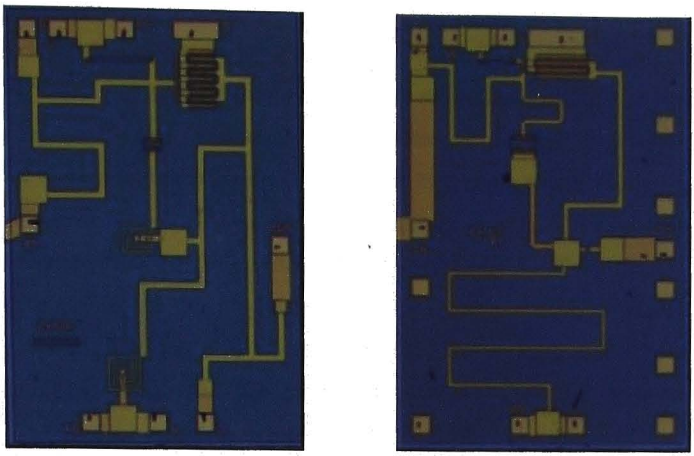
where, $I_m$ is the peak current of the device. For a 900μm MESFET, considering the typical values of $I_m$ =150mA, $V_b$ (breakdown voltage)=10V, $V_p$=2.3V and $V_{knee}$=1.1V, the maximum power can be estimated using (3.13) to be

$$P_{out} = (150/8)(10V - 2.3V - 1.1V) \cong 120mW \tag{3.14}$$

In principle, this device can deliver a power of more than 100 mW, but in practice, it is deteriorated by the output conductance of the device ($g_{ds}$). $g_{ds}$ is a combination of the channel resistance ($R_{ch}$) and contact resistance of the source and drain contacts. In the present configuration, a cascade of MMICs is used to drive the final MMIC to deliver the desired output power of 20dBm. The final MMIC '24106F', shown in figure 3.30a, was selected and studied for its RF output power performance before and after correction of the alloy process. The output power of batch # 205, processed prior to alloying optimization, was in the range of 18 to 19.88dBm. 'Under-alloy' batches typically yielded very few working MMICs with the desired power output. Batch # 224 and # 246 were processed after ohmic alloy optimization. Output power of B # 224 and # 246 were between 19.35 to 22.2 dBm, and 19.5 to 22.53 dBm, respectively. The yield of these batches was also very high. The plot of $R_c$ versus $P_{out}$(min) of these batches is shown in figure 3.31.

'24103E' was another medium power amplifier in the chain (figure 3.30b), was also analyzed for its RF performance. The power output dependence on $R_c$ for this MPA also was similar to the '24106F'.

While the gain of the amplifier primarily depends on transconductance of the device, the output power is a complex function of transconductance, output conductance, and the ohmic contact resistance of the source and drain contacts. Influence of low resistance contacts on the RF performance of the MMICs, especially the power output, was evident from the graph of $R_c$ vs. $P_{out}$.



(a) (b)

**Figure 3.30. The medium power amplifiers of the X-band MMIC chain (a) final stage of MPA chain, 24106F, and (b) another MPA of the chain, 24103E**

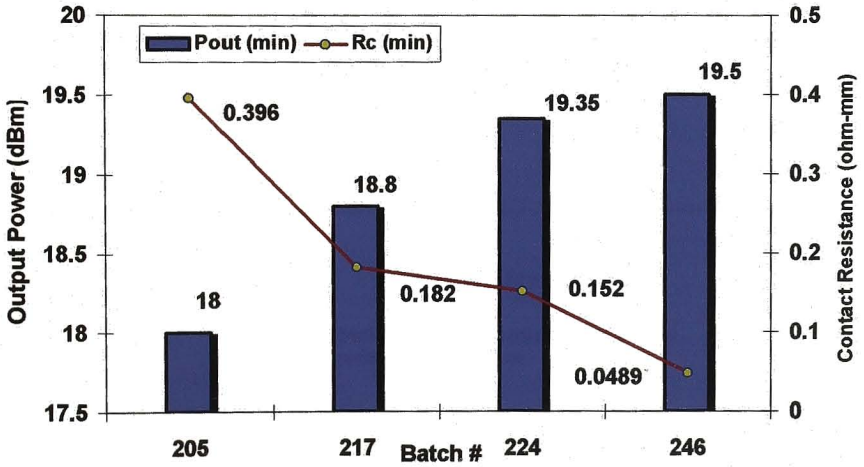



**Figure 3.31. Dependence of output power on contact resistance for '24106F' MPA.**

### 3.2.5. Reliability and contact stability

#### 3.2.5.1. Accelerated temperature aging

Accelerated aging tests were conducted at three different temperatures, viz , 185°C, 200°C and 230°C, on different sets (of 12 structures each) of assembled TLM structures for 4000 hrs each. In practice, an occurrence of a drift of at least +20% in the value of $R_c$ as a failure criterion is chosen for evaluation of life. During this study also, a +20% drift in the 'final $R_c$' value was initially chosen as the criterion It was noticed that even after 4000 hrs, there were no occurrences of any drift of +20%. Drifts of only +10 to +13% had occurred during the course of experiments Hence, for the purpose of calculations, drift values near +13% were treated as failures of +15% for obtaining the worst-case life estimation analysis Drifts of 10% were also compared in order to ascertain if the contact degradation mechanism was due to a single mechanism [15]. Therefore, the failure time $t_F$ was defined as that time at which 'final' $R_c$ increased by factors of +10% or +15% from the value prior to tests.

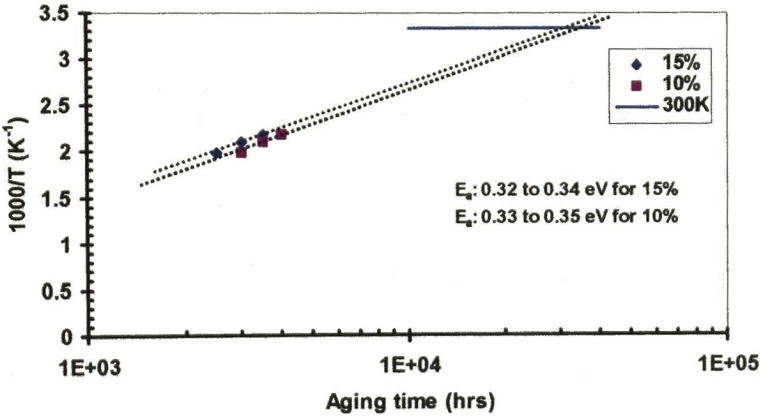



**Figure 3.32. Arrhenius activation energy plots of inverse of absolute temperature vs. failure time.**

Figure 3 32 is a plot of natural logarithm of the failure time against the inverse of absolute temperature. The experimental plots of +15% as well as +10% drifts have resulted in straight lines. Extrapolation to 300K reveals the operating life of the contact. As per this graph, the estimated life would be about 30,000 hrs or longer for drifts of +10 to +15%. The activation energies range between 0.32 to 0.35eV. This

estimation has considered only very low values of drift since drifts more than +15% could not be obtained in any of the TLM structures. In principle, even a drift of +20% also does not cause any appreciable change in the RF characteristics of MESFET [16]. Therefore, consideration of +10 to +15% drifts is highly severe, and practically, life of the contacts would be much longer if we consider drifts of +20%. This showed that the contacts were extremely reliable and thermally stable. This is possibly one of the lowest drifts reported in literature, to the best of our knowledge [17].

### 3.2.5.2. Thermal stability

The reasons for the thermal stability of contacts were further explored. The above results indicate that the contacts have shown minimum degradation even after subjecting the TLM structures to 4000 hrs of accelerated thermal aging tests.

As presented in § 3.2.1, the contact resistance of the 'under-alloyed' contacts increased from the initial spread of 0.12–0.16 Ω-mm to very high values of 0.4–0.7 Ω-mm at the final level. This change in the $R_c$ value occurs after alloying during further device processing, and is not the drift discussed as the failure criterion in the previous subsection. On the other hand, the distribution of initial $R_c$ of the optimum alloyed contacts was 0.05–0.07 Ω-mm and increased only to a maximum of about 0.2 Ω-mm at the final level. As mentioned earlier, the wafers undergo different heating cycles during device processing after the alloying step. Dehydration baking cycles at 200°C for a cumulative time of more than 200min., baking prior to dielectric nitride deposition processes at 250°C for a cumulative time of 60min., curing of the polyimide film at 330°C for a time of 45min., resist hard baking at 120°C for a cumulative time of 180min., and stabilization baking at 280°C for a duration of 60min., are the major heating cycles that the wafers undergo cumulatively. Figures 3.3 and 3.4 show the differences between the 'under-alloyed' and optimally alloyed contacts at the 'initial' as well as the 'final $R_c$' stages. The thermal stability of the optimally alloyed contacts is apparent from these distributions. While, the 'initial $R_c$' values of the optimally alloyed contacts have approximately doubled at the 'final' level, they are still very low in the range of 0.15-0.20Ω-mm. Whereas, it increased more than four times and has very high values unsuitable for device operation for the 'under-alloyed' contacts. In order to understand the reasons for thermal stability, typical samples at the 'final $R_c$' stage (from both the conditions) were backside SIMS

profiled. The 'initial $R_c$' of optimally alloyed sample was 0.06 Ω-mm and the 'final $R_c$' was 0.13 Ω-mm. A small decrease of concentration of Ge at the surface was observed, as shown in figure 3.33. Any decrease of surface concentration of Ge would increase the sheet resistivity of the 'reacted' GaAs region near the surface. Simultaneously, Au and Ni are seen to diffuse further into the channel region. Ni has diffused about 1500Å and Au was found deeper at about 1700 Å, within the channel. This deeper penetration of Au would result in the formation of AuGa compounds, but as Ge shows lesser diffusion comparatively, the remaining unfilled Ga vacancies could cause the increase of sheet resistivity. However, this additional diffusion is small and has not caused any major changes in the 'final' $R_c$ values of the optimally alloyed contacts.

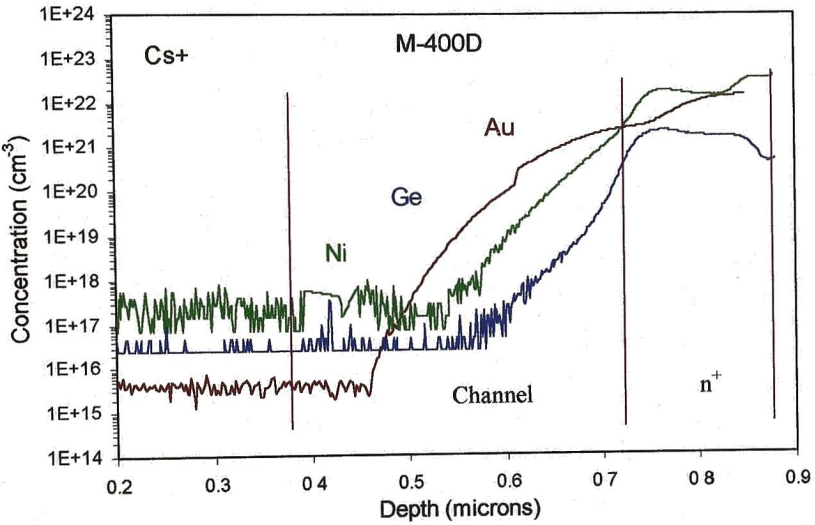



**Figure 3.33. Backside SIMS profile of optimally alloyed contacts at 'final' $R_c$ showing a reduction in the surface concentration of Ge. Diffusion of the alloy materials is also noticeable.**

Another typical sample of the 'under-alloy' case at the 'final $R_c$' stage was backside SIMS profiled (figure 3.34). It can be seen that there is an anomalous diffusion of Ni deep into the channel, and even into the semi-insulating substrate. It is also noticeable that Ge and Au have diffused far more into the channel region. The concentration of Ni also is very high in these regions compared to the profiles of Au and Ge. The incoherent diffusion of alloy materials deeper into the substrate is due to

the cumulative heat treatments during device processing. Hence, the contact resistance had deteriorated to a very high value.

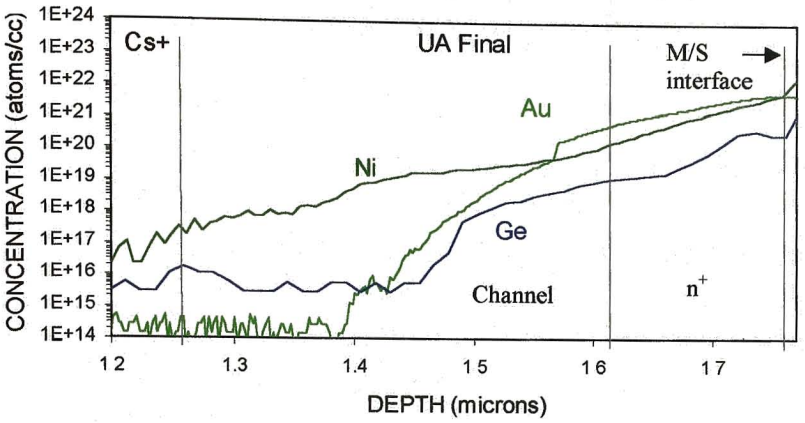



**Figure 3.34. Backside SIMS of the 'under-alloyed' sample at the 'final $R_c$' stage showing anomalous diffusion of ohmic material.**

In spite of interdiffusion, due to very high Ge concentrations in the $n^+$ layer, the contact resistance did not increase. Ge concentration at the $n^+$-n interface in the channel region still is retained at a very high level Formation and uniform occupation of the thermally stable Ge-rich compounds during optimum alloying are possibly the reasons for the thermal stability of the low resistance contacts formed during these experiments [7, 18]. This explains the low drift percentages during aging studies.

### 3.3. Conclusions

From the above results, important aspects of low resistance contact formation to MESFETs have been understood. For achieving low contact resistances, the most critical condition was the indiffusion of Au, which forms AuGa compounds in the diffused regions. Presence of these compounds along the depth enabled the formation of Ni-rich compounds, which assisted Ge indiffusion and doping. These compounds were dominantly present in the diffusion region of the optimally alloyed sample.

Higher doping of $n^+$-layer is only a necessary condition, but not sufficient to obtain low contact resistances. Additional doping of the $n^+$-n interface and the channel region to about 1000Å is the sufficient condition to achieve low contact resistances

This modified the access region with the creation of a low resistance path for current flow.

A correlation between the surface morphology and contact resistance has been established. Low resistance contacts with lower surface roughness were obtained.

The optimized contacts were thermally stable and reliable.

### 3.4. References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# Chapter IV

## Influence of implant activation on ohmic contacts

*Annealing experiments on ion-implanted MESFET wafers were performed to activate Si implants. The wafers were characterized by SIMS, C-V profiling and Hall, and percentage of activation was estimated. Implant activation of $n^+$ and channel layers are correlated to formation of low contact resistances. The results are presented and discussed.*

### 4.1. Introduction

Rapid thermal annealing experiments were performed between 925°C and 955°C to determine the lowest sheet resistivity ($\rho_{sheet}$). Annealing below 925°C resulted in very high and inconsistent $\rho_{sheet}$ values higher than 220Ω/□. Above 955°C, the encapsulant film deteriorated leading to arsenic outdiffusion. Table 4.1 gives the details of the annealing experiments at a fixed time of 15 sec. Table 4.2 gives the details of annealing experiments at 945°C and 955°C for different anneal times.

Table 4.1. Annealing experiments at 15 sec

| Temperature (°C) | Time (sec) | $\rho_{sheet}$ (Ω/□) | Mobility ($cm^2$/V sec) |
|---|---|---|---|
| 925 | 15 | 202 | 2050 |
| 935 | 15 | 192 | 2130 |
| 945 | 15 | 188 | 2390 |
| 955 | 15 | 173 | 2640 |

Table 4.2. Annealing experiments at 945°C and 955°C

| Temperature (°C) | Time (sec) | $\rho_{sheet}$ (Ω/□) | Mobility ($cm^2$/V sec) |
|---|---|---|---|
| 925 | 35 | 163 | 2340 |
| 945 | 20 | 186.7 | 2980 |
| 945 | 25 | 184 | 3000 |
| 945 | 30 | 186 | 2630 |
| 955 | 20 | 169.4 | 2920 |
| 955 | 25 | 162.5 | 3030 |
| 955 | 30 | 177.4 | 2610 |

Few wafers were implanted with higher implant doses of $2.5 \times 10^{13}$ ions/$cm^2$ and $7 \times 10^{12}$ $cm^{-2}$ for the $n^+$ and channel, respectively, for the purpose of studying the

role of higher concentrations on contact resistance. They were processed upto ohmic contact formation.

Very low values of $\rho_{sheet}$ of about 160Ω/□ were obtained for annealing at 955°C for 25 seconds with a standard deviation of 2.5-3.5%. High values of Hall mobility, about 3000$cm^2$/V sec, were also obtained for the 955°C /25 seconds cycle (table 4.2).

## 4.2. Results and discussion

### 4.2.1. SIMS studies

In order to correlate the Si doping concentration to contact resistance (which is related to alloying), SIMS profiling was performed on the above wafers. The peak concentrations of the $n^+$ and the channel regions of the profiles of different anneal cycles were compared to understand the changes in their profiles. The 'tail' regions of the channel implant of these anneal cycles were also compared for understanding the depth of diffusion. It was observed that when diffusion is deeper in the tail portion, the peak channel concentration drops down, indicating lower activation of the channel implant.

The SIMS profile of the as-implanted wafer is shown in figure 4.1. The peak $n^+$ concentration was about 3 x $10^{18}cm^{-3}$, while the peak channel concentration was about 3 x $10^{17}cm^{-3}$. Figure 4.2 shows SIMS profiles of anneal cycles of 925°C and 955°C for 15 sec. A minor difference in the peak and the tail regions was noticeable, and the profile of 955°C showed a higher peak channel concentration and a reduction in tail. Eventhough the differences were small, the tendency for increase in peak carrier concentration with anneal temperature was noticeable.

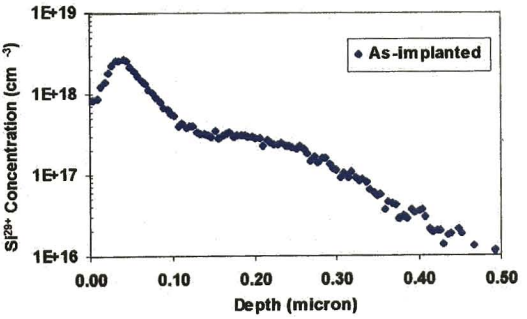



Figure 4.1.SIMS profile of as-implanted wafer

SIMS profiles of wafers annealed at 955°C for durations between 20 to 30 seconds are shown in figure 4.3. The channel profile of 25sec annealing showed a reduced tail as well as higher peak concentration. 30 sec annealing showed deeper

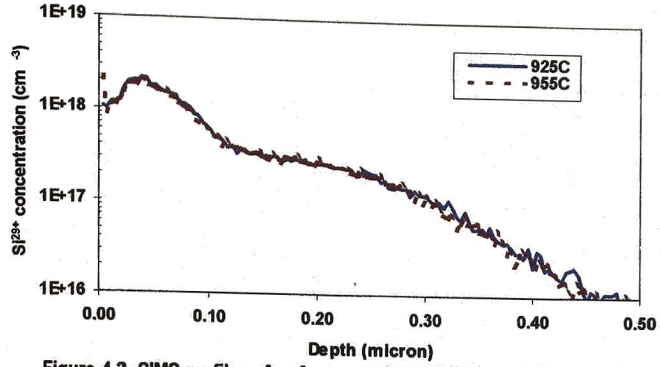



**Figure 4.2. SIMS profiles of wafers annealed at 925°C and 955°C for 15 sec, showing improvement with increasing temperature.**

diffusion in the tail region and reduction in peak channel concentration. Maximum peak $n^+$ concentration and maximum peak channel concentration were observed only for the anneal cycle 25 seconds.

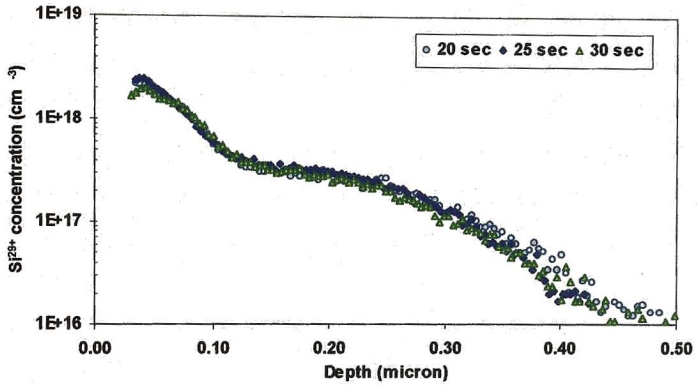



**Figure 4.3. SIMS profiles of annealing at 955°C for different times.**

The above results have shown that peak carrier concentrations of the $n^+$ as well as n regions have concurrently occurred for 25 sec at 955°C. Temperatures below 955°C do not show any appreciable increase in the $n^+$ and the channel concentration areas. When compared to the as-implanted Si profile, the increase of the peak carrier concentration of the channel is quite high and activation seems nearly complete. The peak of the $n^+$ layer is still lower than the as-implanted wafer, indicating the lower levels of activation of the surface layer implanted at lower energies.

### 4.2.2. Capacitance - voltage profiling

The activated dopant distributions were obtained from electrochemical C-V

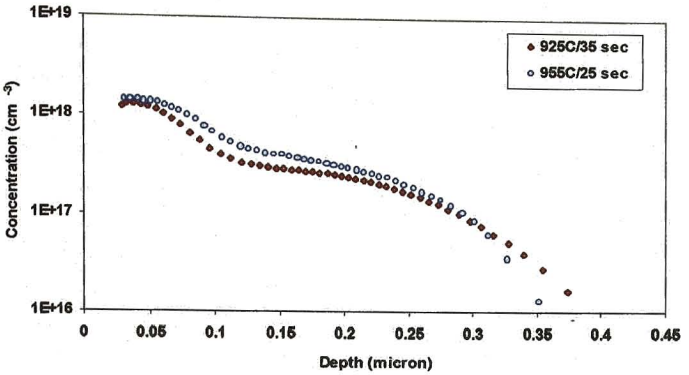



**Figure 4.4. Comparison of electrochemical C-V profiles of 925°C/35sec and 955°C/25sec cycles**

profiling. C-V profiles of the wafers annealed for 15 seconds show no significant improvement in their peak concentrations. A larger spread of dopants is observed for annealing durations of 30 sec and longer, as shown for annealing at 925°C for 35 sec in figure 4.4. Maximum increase in peak carrier concentrations of the $n^+$ as well as channel layers is noticeable for the optimum anneal cycle. The characteristics of the C-V profiles match with the SIMS profiles. The reduction in 'tail' region has raised the plateau or peak concentration region of the channel

### 4.2.3. FATFET C-V profiling

The channel doping profiles of the annealed wafers were also verified by electrical C-V profiling on fabricated FATFETs in the annealed wafers. Figure 4.5 shows the comparison of FATFET profiles of the optimum anneal cycle with

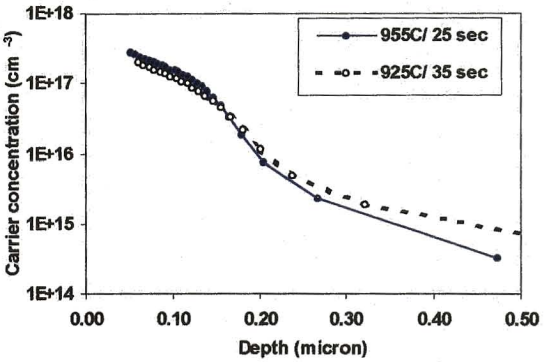



**Figure 4.5. FATFET C-V profiles of 925°C/35 sec and 955°C/25 sec anneal cycles.**

the cycle of 925°C/ 35 sec. The shallower tail portion and the higher channel peak are clearly observed for annealing cycle of 955°C/ 25 sec. A complementary behaviour is noticed clearly for the 925°C/35 sec cycle. This clearly reiterates the improvement in activation of the 955°C /25 sec anneal cycle.

### 4.2.4. Activation

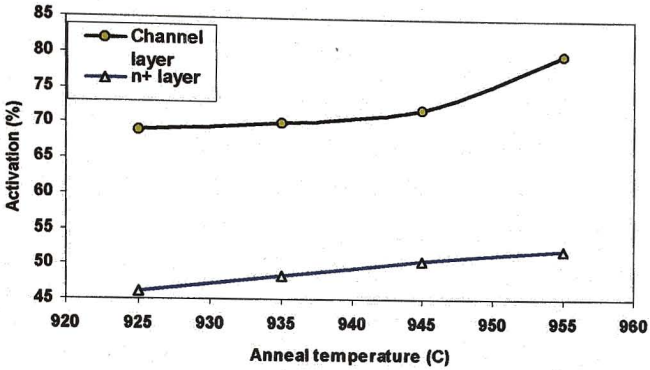



**Figure 4.6. Percentage of activation at different annealing temperatures for annealing time of 15 sec.**

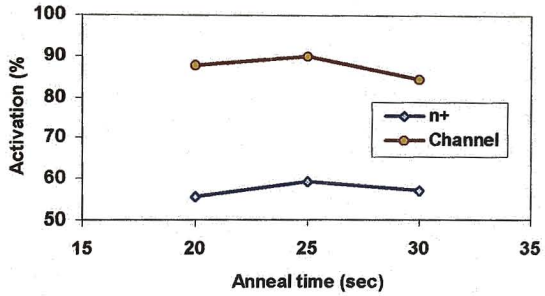



**Figure 4.7. Percentage of activation for different anneal times at 955°C**

The percentage of activation of an anneal cycle was estimated from comparing the electrochemical C-V profile with the SIMS profile. Figure 4.6 shows the percentage of activation at different anneal temperatures for 15 sec anneal time. Activation of both the $n^+$ as well as n layers are seen to increase with anneal temperature. The activation trend at 955°C for different anneal times is shown in figure 4.7. The percentage of activation of the peak channel region and $n^+$ region are higher for 25 sec anneal time at 955°C. About 85% of the channel implants, and 60%

of the $n^+$ implants were activated for this anneal cycle. Maximum levels of activation for both the $n^+$ and the channel layers have occurred simultaneously only for this anneal cycle. But, for the anneal cycle of 925°C/35 sec, the $n^+$ activation was found to be higher compared to the channel region.

### 4.3. Ohmic contact resistance

The above wafers from the annealing experiments were processed further and ohmic contacts were fabricated using the optimized alloy cycle of 400°C for 150sec (discussed in § 3.2.1). The contact resistance ($R_c$) was observed to decrease with activation annealing temperature (figure 4.8), and the lowest values of about 0.06Ω-mm were obtained for annealing at 955°C. The consistency of occurrence of very low values was higher at this annealing temperature. The dependence of $R_c$ on activation annealing temperature for the high dose wafers (2.5 x $10^{13}$ ions/cm$^2$ and 7 x $10^{12}$ cm$^{-2}$ for the $n^+$ and channel, respectively) is also shown in figure 4.8 along with the trend for the regular doses of 1.5 x $10^{13}$ ions/cm$^2$ and 6 x $10^{12}$ cm$^{-2}$. The $R_c$ values were about 0.05Ω-mm for 955°C. This experiment directly confirms the role of increased carrier concentration on $R_c$.

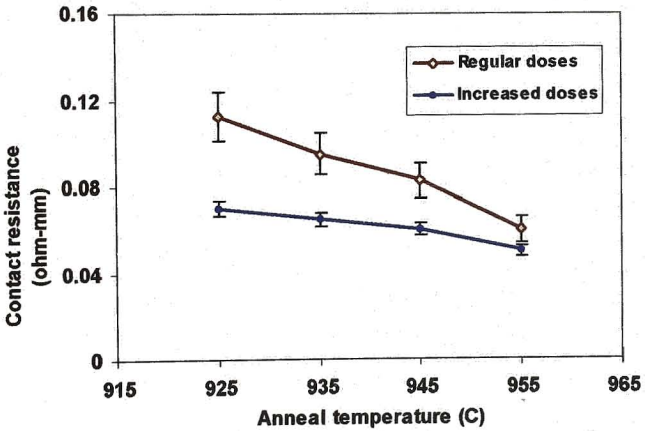



**Figure 4.8. Dependence of contact resistance on annealing temperature for different implant doses.**

It was found that corresponding to the occurrence of low $R_c$ in optimally activated wafers, higher peak carrier concentrations of $n^+$ and channel layers were also observed. It is clear that the simultaneous occurrence of high peak carrier

concentration in both the layers seems to be the critical condition for achieving very low contact resistances.

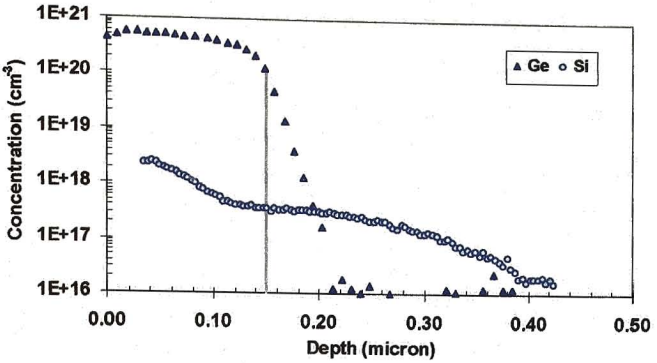



**Figure 4.9. SIMS profiles of Si and Ge superimposed to highlight the increase of concentration in the $n^+$ and the $n^+$-n interface regions.**

Backside SIMS profiling of the ohmic contacts in the samples with optimum alloying was carried out to understand the nature and extent of germanium indiffusion (sample discussed in § 3.2.2.1). This revealed two important facts: firstly, the necessity of a degenerate Ge doping of the entire depth of $n^+$ contact layer, and secondly, the importance of highly doping the channel to a depth of about 0.1μm [1]. The increase in $n^+$ layer concentration reduced the effect of metal-semiconductor barrier. Whereas, the flow of current into the channel is enhanced only by the increase in peak channel concentration. A superimposed plot of SIMS profiles of the optimally activated Si and optimally alloyed Ge (present in the ohmic contact metallisation) shows the high levels of concentrations of Ge at the metal-semiconductor interface, the entire $n^+$-layer, and more importantly, at the '$n^+$-contact layer-n-channel layer' interface (figure 4.9). We can assume that the $n^+$-n interface is a homojunction of layers with concentrations of $10^{18}cm^{-3}$ to $10^{17}cm^{-3}$, respectively (figure 4.10) Current flow through this transition from a high concentration layer to a low concentration layer faces a resistive region at this 'interface', and this resistive element is bound to dissipate electrical energy [2]. The rate of energy loss or the power (P) used up, is the resistance (R) times the average square of current (I), and is written as [3]

$$\langle P \rangle = R\langle I^2 \rangle = R \cdot \tfrac{1}{2} I_0^2 \qquad (3)$$

This energy goes into heating the resistive region, called the heating loss or the Joule heating. In the case of lower activation, this resistance of the $n^+$-n interface region limits the contact resistance, and current flow into the channel is predominantly thermionic [4]. Maximizing activation of the channel implant reduces this phenomenon. High doping of this $n^+$-n interface can be also thought of extending the degenerate conduction band into the channel. Therefore, the role of increasing the carrier concentration of the $n^+$-layer and the peak region of the channel implant seems to be that of establishing a direct contact to the channel from the ohmic contact pads. This ultimately reduces the contact resistance and the resistance of the access region as well. Reduction in both the resistances has been responsible for improvement in device performance.

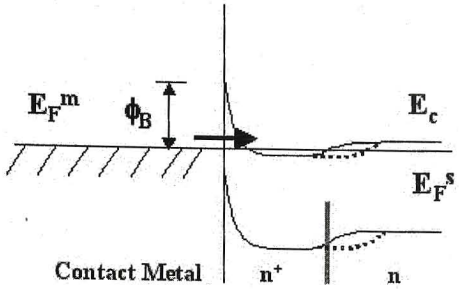



**Figure 4.10. The $n^+$-n interface gets altered due to (dotted line) high channel activation and degenerate doping as a result of optimum alloying, during ohmic contact formation subsequently.**

## 4.4. Influence on electrical parameters

### 4.4.1. D. C. characterization

The wafers from the above experiments were processed together and their DC electrical characteristics were studied. Duration of mesa etching while forming mesas was observed to understand the 'tail' region of the channel implant profile. The completeness of etching was confirmed by the occurrence of higher mesa-to-mesa isolation voltages. This was compared with pinch-off voltage and transconductance values of the fabricated MESFETs. For an effective comparison of the parameters of mesa etching time, $g_m$, and $V_p$, wafers annealed with 925°C/35 sec cycle were processed together with other wafers.

#### *4.4.1.1. Mesa-to-mesa isolation*

For wafers annealed at 955°C for 25 seconds, mesa etching was completed in about 7.00 min. For 945°C, it was achieved in 7.30 min. For the annealing cycles of

925°C and 935°C, and for anneal cycles with longer duration, etching time was longer by about 2 minutes. Mesa-to-mesa breakdown voltages were consistently observed to be greater than 50V at 1 μA for the annealing cycle of 955°C for 25 seconds. For wafers with longer anneal durations of 30 and 35 seconds, isolation could not be achieved completely, and the breakdown voltages were about 40V. The lower etching time and high isolation voltages for the 955°C for 25 sec cycle clearly indicate the reduction in 'tail' of the carrier concentration profile.

#### *4.4.1.2. Pinch-off voltage and transconductance*

Figure 4.11 shows the pinch-off voltages at different source-drain currents of the devices fabricated from the wafers annealed with the cycles of 955°C for 25 sec and 925°C for 35 sec. Linearity in pinch-off voltages with respect to the source-drain current was observed. The maximum voltages of the 955°C for 25 sec anneal cycle were -2V. It was observed that $V_p$ of 955°C /25 sec cycle were lower by at least 0.3V, compared to the 925°C /35 sec cycle.

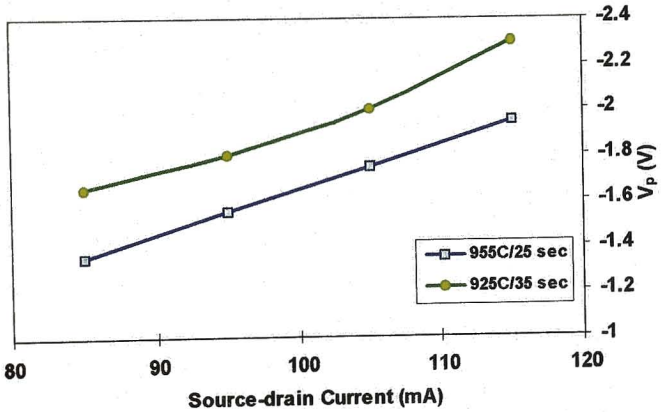



**Figure 4.11. Pinch-off voltages for 925°C/35 sec and 955°C/25 sec cycles at different source-drain currents**

Transconductance of the 1 x 150 μm devices was in the range of 17–21 mS for wafers annealed with 925°C/ 35 sec cycle (and contacts were 'under-alloyed' in this case). $g_m$ improved to a range of 19–23 mS with optimization of the alloy cycle. After optimization of the activation annealing process, $g_m$ values were consistent at 22–25mS (figure 4.12). The four-finger or 600μm MESFET also exhibited similar trend in their characteristics.

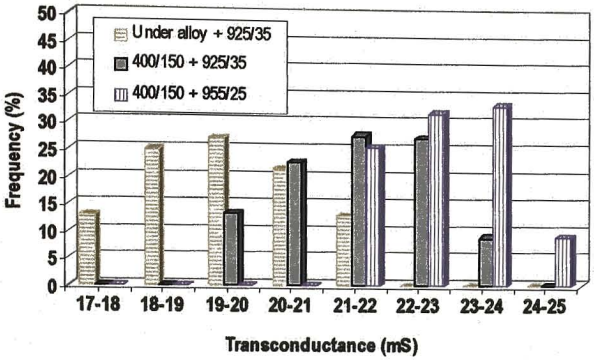



**Figure 4.12. Increase in transconductances of 1 x 150μm MESFETs with increase in activation. Effect of optimal alloying is also shown for comparison.**

The $V_p$ and $g_m$ values showed a clear complementary behaviour proving that the reduction in 'tail' has influenced the peak carrier concentration of the channel layer. This is again consistent with the data obtained after mesa etching. The increase in $g_m$ for the 955°C for 25 sec cycle coupled with optimized alloying shows that the activation process has benefited the device characteristics.

### 4.4.2. RF characterization

600μm MESFETs with 0.7 μm gates fabricated on the optimally activated wafer showed cut-off frequencies ($f_t$) greater than 18.5 GHz, and RF gain ($S_{21}$) in the range of between 4.0–4.2 dB at 12 GHz. These are superior to the performances from the wafers annealed with the cycle of 925°C/ 35 sec. The $f_t$ values were about 17.0 to 17.5 GHz, and $S_{21}$ was approximately 3.5dB, pointing to lower activation. The occurrence of higher RF gain and $f_t$ as a result of increase in transconductance shows the influence of activation.

## 4.5. Conclusions

Low sheet resistivities of 160Ω/□ were achieved for the optimum anneal cycle of 955°C for 25 sec. Maximum activation of about 60% and 85% were simultaneously obtained for the $n^+$ and channel implants, respectively, for this anneal cycle. It was also observed that the 'tail' region of the channel implant was shallow and peak concentration region was higher. This was validated by lower pinch-off voltages and high transconductances.

The ohmic contact resistance was observed to decrease with annealing temperature and was lowest for optimum annealing at 955°C with values of 0.06 Ω-mm. Increase in the concentration of the peak region of the channel favoured the reduction of the resistance of the $n^+$-n interface. This minimized the possibility of Joule heating at this interface. When wafers with high activation were optimally alloyed, the $n^+$-n interface gets degenerately doped enabling direct current flow into channel. Contact resistance was thus dependent on the reduction in the resistance of the $n^+$-n interface region. Very high concentration of the $n^+$-layer seems to be the necessary condition and not the sufficient condition for achieving low contact resistance. It was found that very high carrier concentrations of both the $n^+$ as well as channel layers were responsible for low contact resistances, which we feel should be the sufficient condition.

## 4.6. References


1. G. Sai Saravanan, Mahadeva Bhat. K, Sandeep Chaturvedi, H. P. Vyas, K. Muraleedharan and A. P. Pathak, *communicated to Microelectronics Engineering, (2007).*
2. G. Sai Saravanan, Mahadeva Bhat. K, H. P. Vyas, K. Muraleedharan and A. P. Pathak, *under review, Radiation effects and defects in solids, (2007).*
3. R. P. Feynman, R. B. Leighton and M. Sands, *The Feynman lectures on Physics*, Vol. 1, Narosa Publishing House, New Delhi (2001) 293.
4. P. J. McNally, Solid-St. Electron. 35(12), (1992) 1705.

# Chapter V

## Ohmic contacts to pseudomorphic HEMTs

*Alloying temperature and time were studied for obtaining very low contact resistances to pseudomorphic HEMTs. Contacts were characterized by backside SIMS and TEM The role of AlGaAs in contact formation was investigated. Also, the contact surface morphology was examined using AFM and SEM. The results are presented and discussed.*

### 5.1. Introduction

Alloying experiments were performed between 390°C and 450°C for 45sec, and at 430°C for 30 sec and 60sec to obtain low contact resistances ($R_c$). Table 5.1 describes the matrix of temperature and time experiments, with average contact resistances.

Table 5.1: Matrix of alloying experiments

| Sample | Alloy Temperature (°C) | Alloy Time (sec) | $R_c$ (Ω-mm) |
|---|---|---|---|
| A | 390 | 45 | 0.16 |
| B | 410 | 45 | 0.125 |
| C | 420 | 45 | 0.096 |
| D | 430 | 45 | 0.06 |
| E | 440 | 45 | 0.225 |
| F | 450 | 45 | - |
| G | 430 | 30 | 0.097 |
| H | 430 | 60 | 0.102 |

### 5.2 Results and discussion

#### 5.2.1. Contact resistance

Figure 5.1 shows the contact resistance as a function of alloying temperature. Figure 5.2 shows the $R_c$ values for samples alloyed at 430°C for different durations. The lowest value of contact resistance of 0.047 Ω-mm was obtained for alloying at 430°C for 45 sec. The typical contact resistances were about 0.06 Ω-mm. Surface roughness was present even for samples alloyed at 390°C, as observed under optical

microscope. Due to the deterioration of surface morphology, $R_c$ of contacts alloyed above 440°C could not be reliably measured.

Samples A, B, C and G are referred to as 'under-alloyed' samples, while E, F and H as 'over alloyed', and D as the optimally alloyed sample.

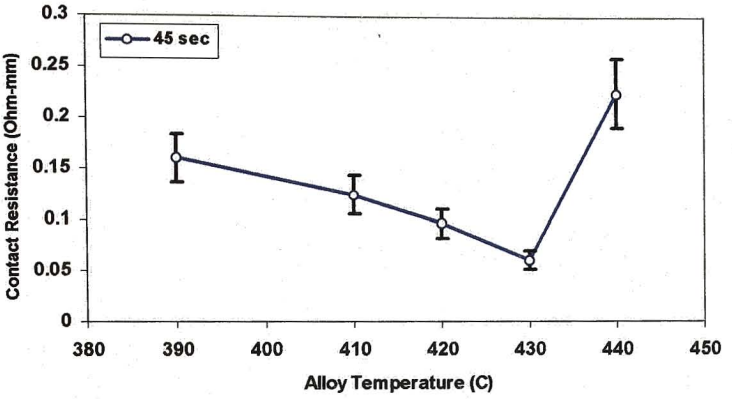



**Figure 5.1. Low $R_c$ obtained for alloying at 430°C for 45 sec. Due to surface roughness, electrical measurements at 440°C were not repeatable.**

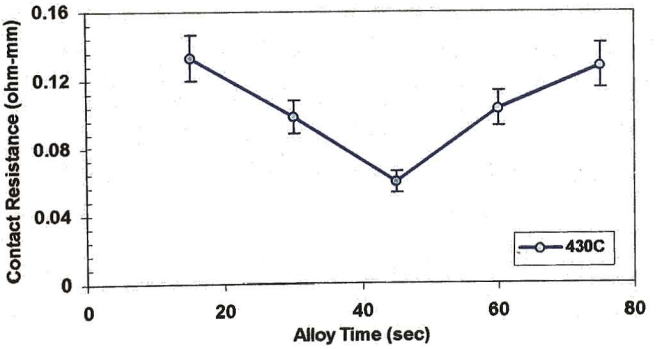



**Figure 5.2. Contact resistance for alloying at 430°C for different durations showing an increase in $R_c$ beyond 45 sec.**

### 5.2.2. Characterization

#### 5.2.2.1. Backside SIMS studies

Ge, Ni and Au concentration profiles have been traced at the following regions of interest in different samples: (i) at the interface between $n^+$-GaAs and ohmic metallisation, (ii) in the AlGaAs layer, and (iii) at the start of InGaAs channel.

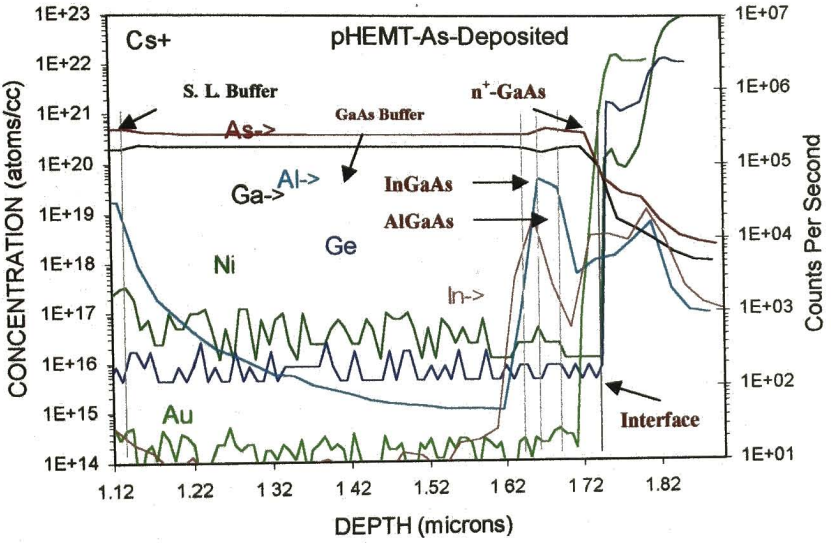



**Figure 5.3. SIMS profiles of as-deposited pHEMT sample**

SIMS profiles of the as-deposited sample are shown in figure 5.3. The device layers are seen along with the buffer layers of semi-insulating (S I.) GaAs, and AlGaAs-GaAs superlattices (S. L.). The ohmic metallisation is on the right side of the graph. Diffusion was not noticed in the metal-semiconductor interface region.

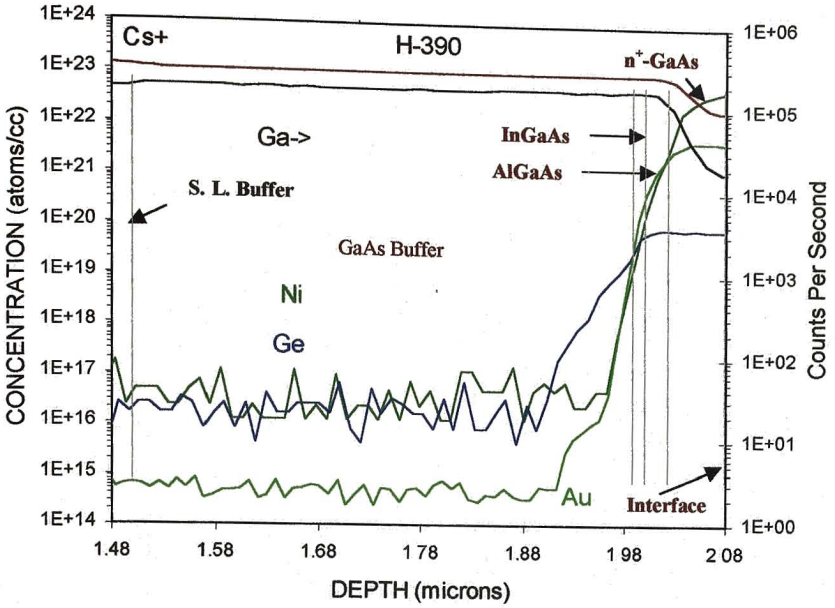



**Figure 5.4. SIMS profiles of pHEMT sample alloyed at 390°C**

In sample A, Ge concentration was in the range of 8 - 9 x $10^{19}/cm^3$ in all the layers, as shown in figure 5.4. From 8 x $10^{19}/cm^3$ in the AlGaAs layers, the concentration reduced to about 6 x $10^{19}/cm^3$ at the end of channel region The concentration levels of Ni were generally above $10^{22}/cm^3$ in the $n^+$-GaAs layer. It reduced from the range of $10^{21}/cm^3$ to $10^{20}/cm^3$ in AlGaAs, and to $10^{19}/cm^3$ in the channel. Au was in the range of $10^{21}/cm^3$ in the $n^+$ region and decreased to $10^{20}/cm^3$ in the AlGaAs layer. Au concentration sloped from 8 x $10^{19}/cm^3$ towards 6 x $10^{19}/cm^3$ in the channel. It was noticed that the alloy materials were able to diffuse into the channel at this alloying temperature of 390°C. In sample B, Ge concentration had increased compared to sample A, and was in the range of $10^{20}/cm^3$. The concentration was nearly uniform throughout the different layers Very high and uniform concentrations of Ni and Au, in the range of $10^{22}/cm^3$ and $10^{21}/cm^3$, were found in all the device layers, respectively. The SIMS profile is shown in figure 5.5.

In sample D, the optimally alloyed sample, a high and uniform Ge concentration in the range of $10^{21}/cm^3$ was observed within the $n^+$- region, as shown in figure 5.6. The concentration was similarly high in the AlGaAs layer and gradually reduced to about 3.5 x $10^{20}/cm^3$ in the channel. In the case of Ni and Au, the

concentration levels were generally above $10^{22}/cm^3$ and $10^{21}/cm^3$, respectively, throughout the device layers. The important factor observed is that the concentrations have reached very high values in the $n^+$, AlGaAs layers, and also in the channel, compared to earlier samples.

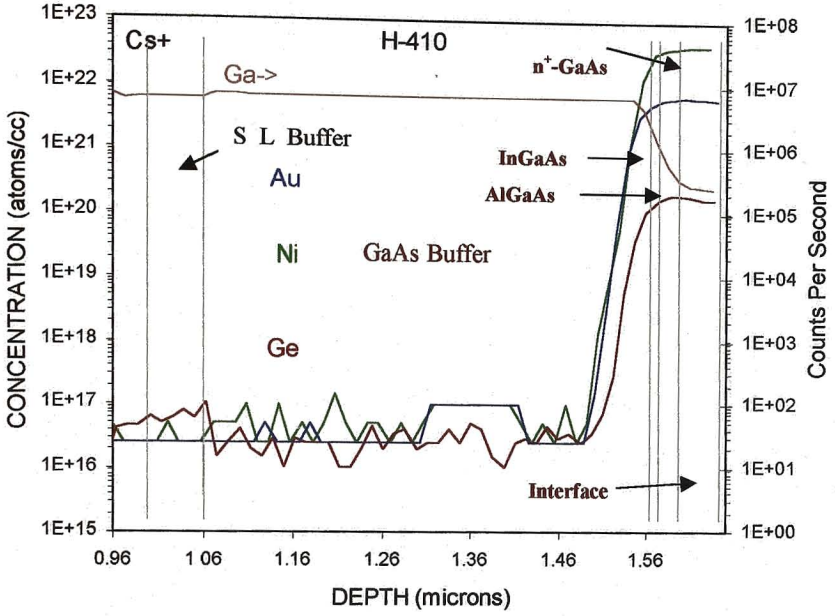



**Figure 5.5. SIMS profiles of sample alloyed at 410°C.**

In sample F, the concentrations have increased further in all the device layers, as can be seen in figure 5.7. While the concentration in the $n^+$ layer and the AlGaAs layer were in the $10^{21}/cm^3$ range, the concentration in the channel was in the $10^{20}/cm^3$ range. The Ni and Au concentrations in all the device layers were in the range of $10^{22}/cm^3$.

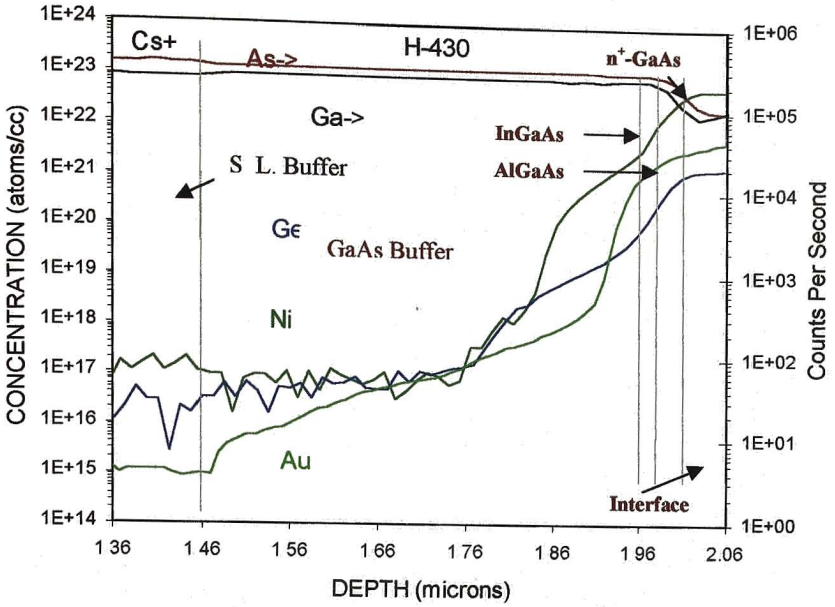



**Figure 5.6. SIMS profiles of sample alloyed at 430°C**

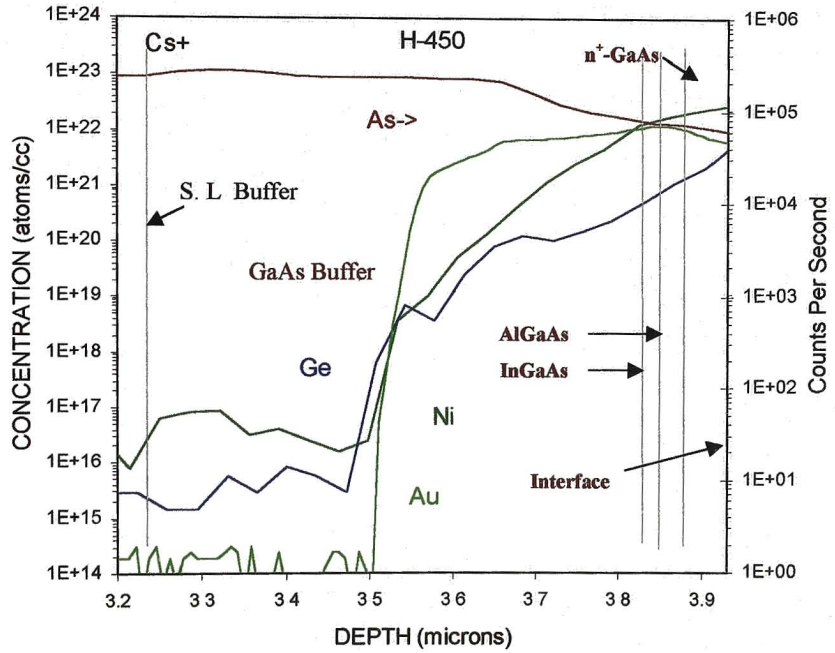
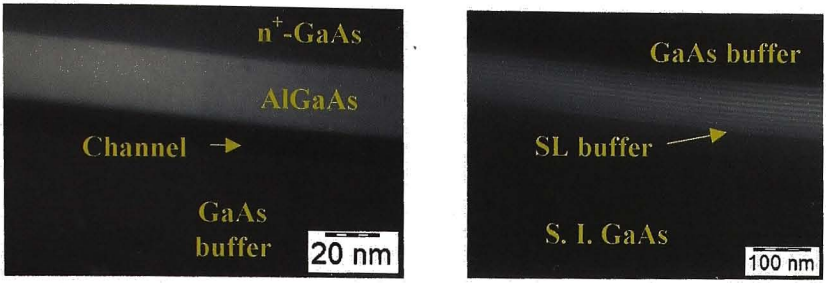



**Figure 5.7. SIMS profiles of sample alloyed at 450°C**

### 5.2.2.2. Cross-section TEM studies

Figure 5.8 shows the cross-section dark field (DF) image of the as-deposited sample, where the layers of $n^+$-GaAs contact, AlGaAs, InGaAs channel, buffer layers consisting GaAs buffer and superlattice buffer of AlGaAs and GaAs quantum wells, are clearly noticeable. The thicknesses of these layers were in agreement with the data from the growth.




(a) (b)

**Figure 5.8. (a) Device layers and (b) buffer layers are seen in the DF images of the as-deposited pHEMT sample.**

In sample B, Au-rich and Ni-rich phases were observed penetrating across the metal-semiconductor interface into the channel (figure 5 9). Both these grain types were nearly evenly distributed. Rough surface morphology of the sample was seen in the bright field (BF) cross-section image in figure 5.10.

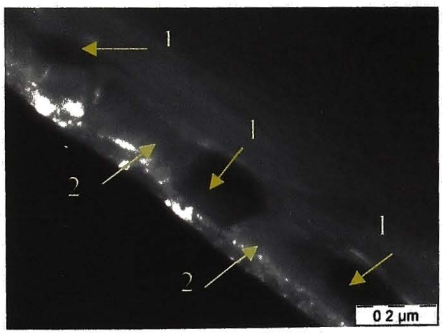



**Figure 5.9. Diffusion grains of the sample alloyed at 410°C. Au-rich and Ni-rich grains are marked as '1' and '2', respectively.**

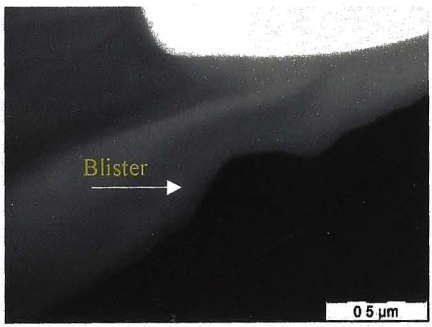



**Figure 5.10. The overlayer showing a large 'blister'.**

A cross-sectional TEM image of sample D (figure 5.11) shows the alloy diffusion into the channel region. The microstructure revealed Ni-rich and Au-rich phases similar to the case of optimally alloyed MESFET sample. Ni-rich phase was found to dominate in the diffusion region. The surface contained protrusions similar to sample B, but their density was less.

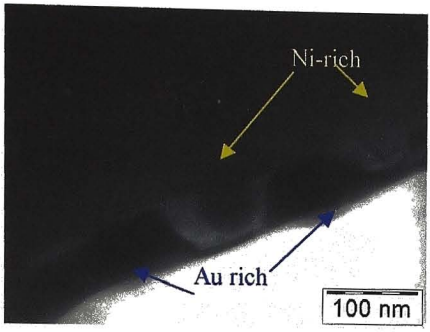



**Figure 5.11. Sample alloyed at 430°C seen with Ni-rich and Au-rich diffusion grains.**

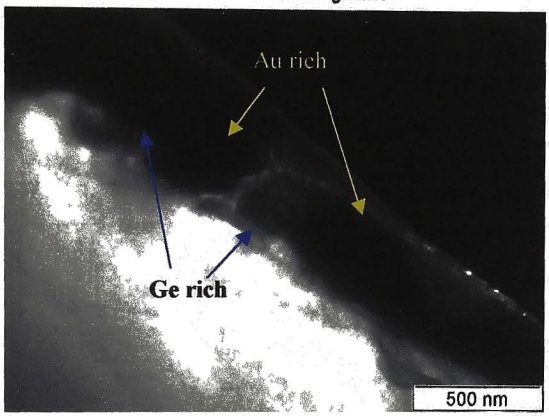



**Figure 5.12. BF XTEM image of the diffusion at 450°C showing Au-rich and Ni-rich diffusion grains.**

The BF image of sample F is shown in figure 5.12. This also contains Au-rich and Ni-rich grains. Au-rich phase seemed to be dominating more compared to the Ni-rich ones. The Au-rich grain sizes were coarser and larger. The overlayer of Au also had large protrusions due to outdiffusion. A typical 'blister' is shown in figure 5.13.

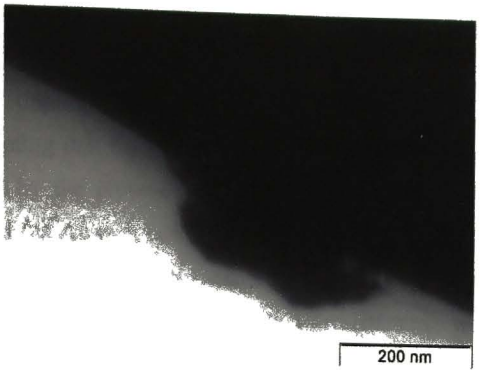



**Figure 5.13. A typical 'blister' on the surface of sample alloyed at 450°C.**

In general, the diffusion front was noticed to be nearly parallel to the interfaces in the case of all the alloyed pHEMT samples.

The Ge diffusion coefficients were calculated using Fick's second law [1]. $D_0$, the diffusion constant was estimated to be $1.71 \times 10^{-11}$ $cm^2/sec$, as shown in figure 5.14. When we compare the pHEMT alloying process with that of the MESFETs, the

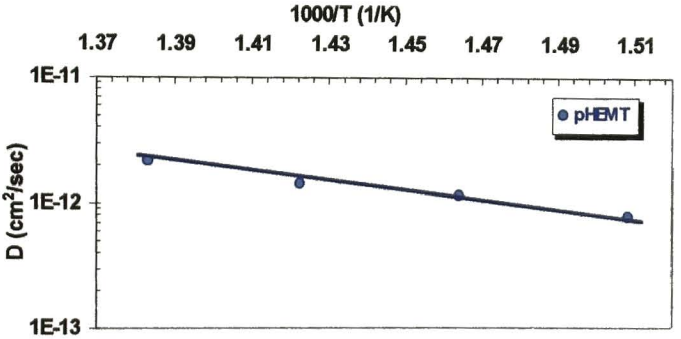



**Figure 5.14. Ge diffusion coefficient vs. $10^3$/T for the pHEMT structure.**

retardation behaviour of the AlGaAs layers can be understood The diffusion constant obtained for alloying of MESFETs, as described in § 3 2.2, was $2.1 \times 10^{-10}$ $cm^2/sec$ It is apparent that diffusion in pHEMT device structures is slower than in MESFET structures, which indicates the influence of AlGaAs layers [2].

We have observed from the SIMS profiles that Au also indiffuses along with Ni and Ge. As a result, Au-rich compounds, such as AuGa, are formed within the semiconductor [3,4]. Presence of these compounds along the depth has favoured Ge in-diffusion and doping [5]. The diffusion mechanism is similar to the case of MESFETs, excepting that the diffusion is slower. Diffusion through this mechanism is also validated by the presence of outdiffused Ga from the surface layers in the overlayer of gold (as Au-rich compounds), as this mechanism is known to primarily depend on the concentration of Ga vacancies.

Ohmic contacts with low contact resistances were observed to be fundamentally dependent on the level of its concentration within different device layers. It is reported that obtaining metal-semiconductor junctions with low contact resistances was possible for high doping levels of the order of $10^{19}/cm^3$ or more [6]. Achievement of very low $R_c$ values for typical MESFET structures was possible at lower alloy temperatures such as 400°C, as these structures consist of only GaAs layers. Whereas, as pHEMT structures possess higher band gap AlGaAs layers, they pose a barrier to the diffusion of alloy materials [7-9]. Direct contact to the channel has been reported to be responsible to reduce the contact resistance and improve the performance of pHEMTs. It is also reported that penetration of alloy materials through AlGaAs layers requires alloying temperatures as high as 430°C or above [7, 9, 10]. Here we have seen that eventhough penetration of alloying materials can be obtained even at 390°C, it does not result in lower contact resistances. In the samples alloyed at 430°C, it is observed from the SIMS profiles that the $n^+$-GaAs region and the AlGaAs layers are doped to very high levels in the range of $10^{21}/cm^3$, respectively. Additionally, the concentration of Ge in the InGaAs channel is seen to increase with alloying temperatures from 390°C to 450°C. The reason for reduction in $R_c$ by more than 60% from 390°C to 430°C probably is the increase in the concentration to $10^{21}/cm^3$ range in the $n^+$-GaAs and the AlGaAs layers. This change, illustrated in figure 5.15, is the threshold for reduction in contact resistance to very low values. Therefore, higher temperatures of 430°C and above are essential for pHEMTs in order to considerably raise the doping levels in order to result in low contact resistances. Above 430°C, surface roughness for this metal system becomes very high, making the electrical measurements difficult.

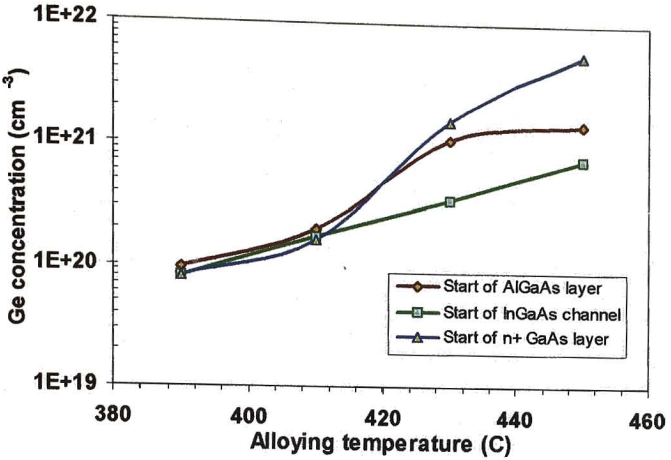



**Figure 5.15. Ge concentration at the start of each layer is shown. At 430°C. the concentration levels have increased by about an order.**

### 5.2.3. Surface morphology studies

#### 5.2.3.1. SEM studies

SEM was used to examine the surface morphology of the 'under-alloy', optimum alloy and 'over-alloy' samples. The surface of the alloyed pHEMT contacts was rougher compared to that of alloyed MESFET contacts. The samples alloyed at 390°C were granular and rough even under an optical microscope. Figure 5.16 shows the typical surface morphology of contacts alloyed at 390°C, 420°C, 430°C and 440°C. The surface of 430°C sample was grainy but looked less rough compared to the earlier samples. In the samples alloyed beyond this temperature, the size of 'blisters' was large and made the surface highly non-uniform.

EDS spectra from the overlayer Au of the above samples are shown in figure 5.17. A gradual increase in the outdiffusion of Ga is observed with temperature. Along with Ga, the sample alloyed at 440°C shows the presence of As also. The 'blister' region on this sample can be seen with even higher amounts of Ga outdiffusion.

The ohmic metallisation was removed by wet chemical etching in order to study the morphology of the 'reacted' semiconductor region. The patterns on the 'under-alloyed' and 'over-alloyed' contacts showed large amount of roughness, while

the sample with the lowest contact resistance was less rough. Figure 5.18(a) shows the reacted GaAs surface of the wafer alloyed at 410°C with varying feature sizes. Figures 5.18(b) shows the sample alloyed at 430°C having uniform feature sizes. Figure 5.18(c) reveals the sample alloyed at 440°C with large features with different sizes and a rough morphology.

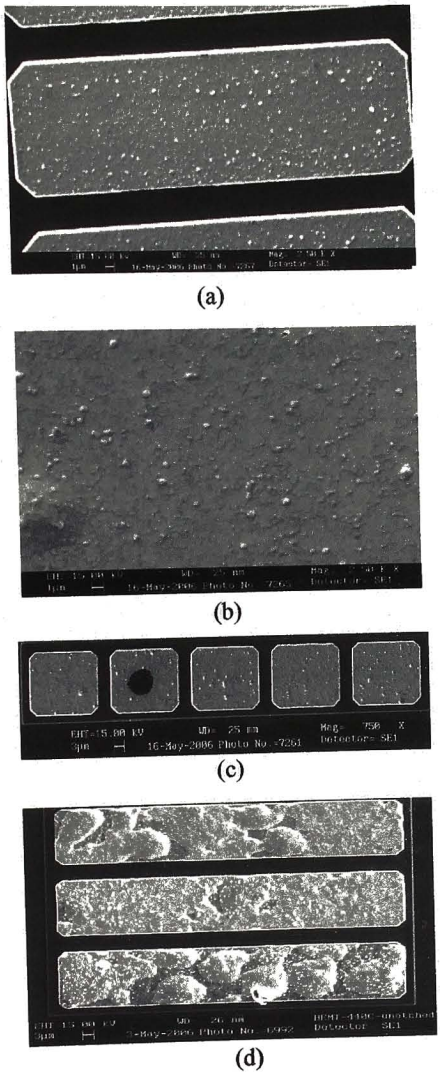



Figure 5.16. SEM images of the contact morphology of samples alloyed at (a) 390°C, (b) 420°C, (c) 430°C and (d) 440°C.

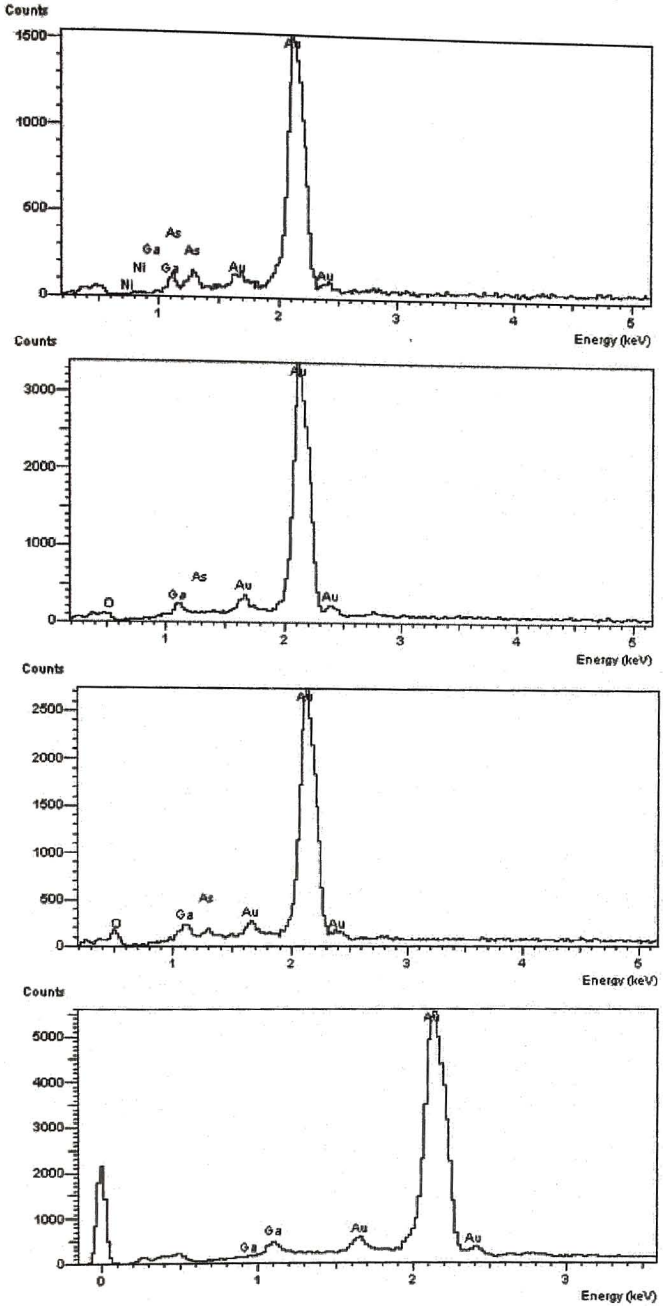
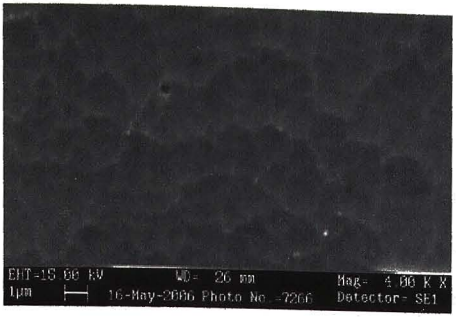
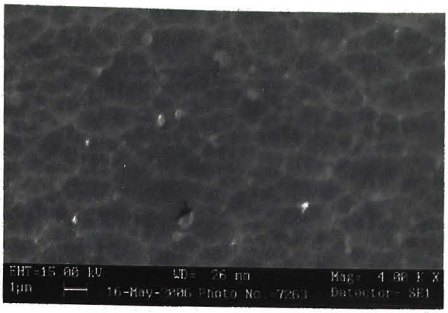


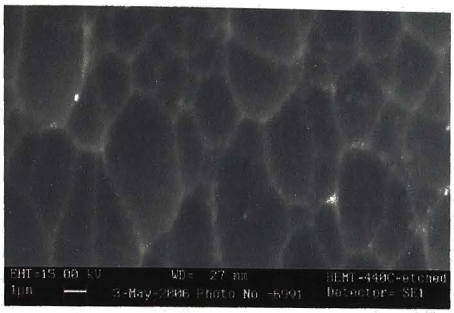

**Figure 5.17. EDS spectra from the overlayers of samples alloyed at (a) 390°C, (b) 430°C, (c) 440°C and (d) 440°C on a blister.**



(a)



(b)



(c)

**Figure 5.18. Etched surface under the contact pads revealing the amount of roughness of the 'reacted' GaAs in (a) 'under-alloy', (b) optimum alloy, and (c) 'over alloy' pHEMT samples.**

### 5.2.3.2. AFM studies

Surface roughness of the selected samples from the three different categories of alloying was studied using AFM. Figure 5.19 shows the AFM images of the ohmic contacts of samples alloyed between 410°C and 440°C. The smoothness of the samples was affected by the presence of protrusions on the surface. Deterioration of the surface due to excessive 'blisters' was clearly noticed at 440°C. Line scan on sample alloyed at 430°C showed better smoothness. The RMS roughness values of the samples at different alloy temperatures are plotted in figure 5.20. The lowest RMS roughness was obtained for the sample alloyed at 430°C. At temperatures above 430°C, the sample surfaces had increasing RMS roughness due to the dominance of 'blisters'. Similar to MESFETs (§ 3.2.3.2), the RMS surface roughness was observed to follow the contact resistance trend with increasing alloying temperature. However, the minimum RMS roughness was higher for pHEMTs.

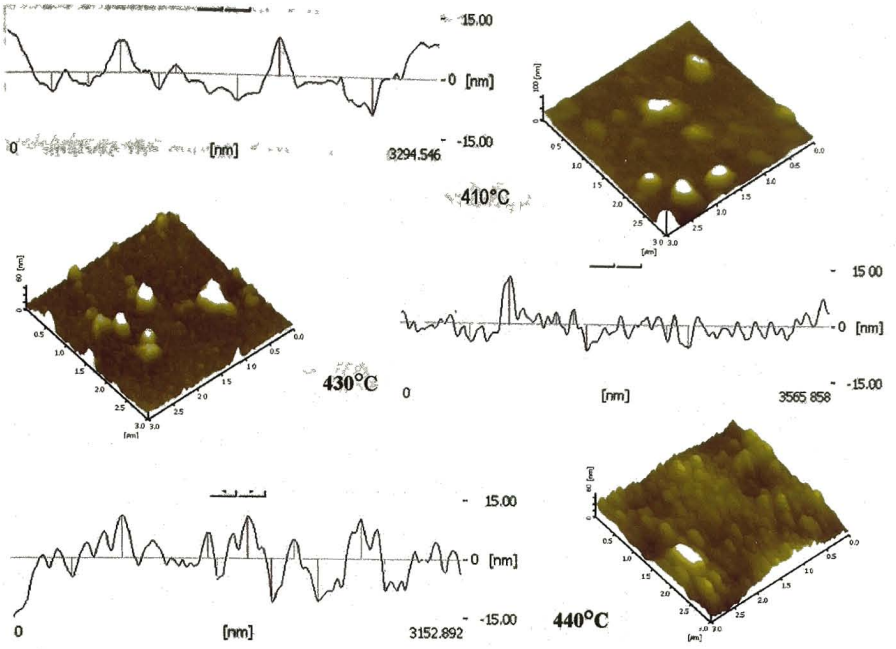



**Figure 5.19. AFM line scans of the contact surface along with images of samples alloyed at 410°C, 430°C and 440°C**

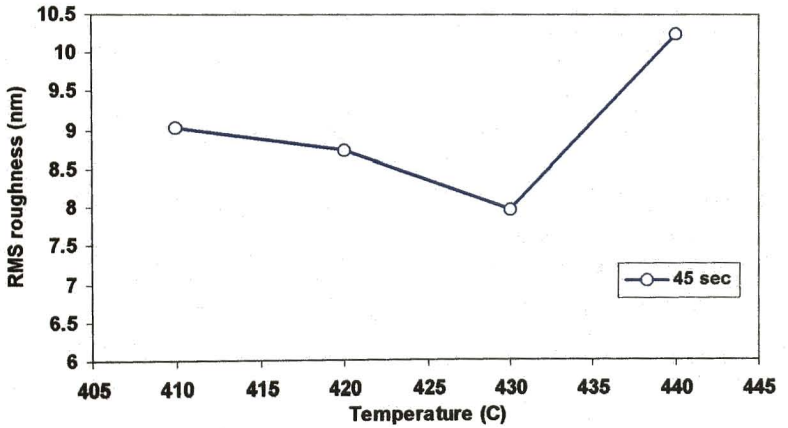



**Figure 5.20. RMS roughness of the contact surfaces vs. alloying temperature of pHEMT samples. The lowest RMS roughness was obtained for 430°C alloying.**

### 5.2.4. Influence on electrical parameters

#### 5.2.4.1. Access resistance

The role of the resistances of different device layers can be resolved when we analyze the current flow path from source to drain, as illustrated in figure 5.21. The resistance of the heterointerfaces can be denoted as $R_{CS}$ and $R_{2DEG}$, referring to the interfaces at $n^+$-GaAs layer–AlGaAs Schottky layers, and the AlGaAs–channel layers, respectively. The individual layer resistances can be denoted as $R_{Cap}$, $R_{Sch}$ and $R_{Channel}$, representing the resistances of $n^+$-cap (contact), Schottky and channel layers, respectively. The AlGaAs layers offer very high resistances, especially as they are undoped. This would be the most dominant factor restricting the current flow. Resistances of both the heterointerfaces also get added to the resistance of the AlGaAs layers. Parallel conduction, occurring along the $n^+$-GaAs and AlGaAs regions

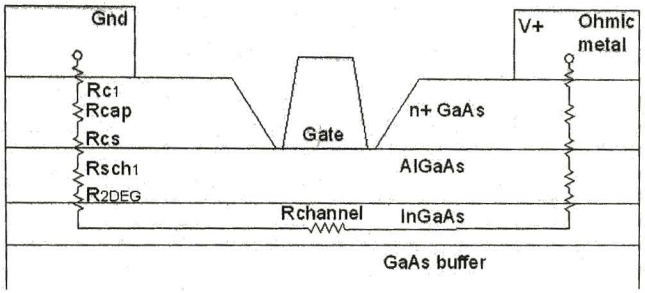



**Figure. 5.21. Current flow path for pHEMTs indicating the resistances of the individual device layers and interfaces. The access region is vertically below the ohmic pads.**

to reach the channel under the depletion region below gate, has been thought of as a probability due to presence of carriers in both the layers (due to background doping, in the case of AlGaAs) [11]. This would arise if the alloy penetration were not deep enough to reach the channel. However, as limited or moderate diffusion of alloy materials into the channel are observed even for low temperature alloying like 390°C during our experiments, the least resistance path for the current flow would be only the region under the ohmic contact pads.

Considering a typical device with the following dimensions: source-drain spacing of 6 μm, ohmic pad dimensions of 100 μm x 30 μm, and, mobility of the

undoped AlGaAs layers as 1800 $cm^2$/V-s, then for the 'under-alloy' conditions the resistance of the 'reacted' AlGaAs layer under the pad would be about 3 x $10^{-3}$ Ω. This would further reduce upon alloying at 430°C to about $10^{-5}$ Ω. On the other hand, the resistance of the conventional access region, $R_{SG}$, between source-gate is described by

$$R_{SG} \approx \frac{L_{SG}}{qNW\mu_0 Z_G} \tag{5.1}$$

where q is electron charge, N is n-type doping density, $\mu_0$ is low-field drift mobility, $L_{SG}$ is the length of region between the source and gate electrodes, $Z_G$ is the gate width and W is channel layer thickness under gate. We can assume a background doping of $10^{16}$ $cm^{-3}$ (n-type). The resistances would then be as high as 3 – 4 kΩ. Hence, lateral conduction would be negligible even for the 'under-alloy' conditions. Therefore, the least resistance conductive path to the channel exists vertically downward through both the heterojunctions. In the optimally alloyed situation, the 'reacted' regions under the pad would be degenerately doped.

The access resistance, now representing only the current flow vertically below a pad, can be formulated as follows:

$$R_{access} \approx R_C + R_{Cap} + R_{Sch} + R_{CS.} + R_{2DEG} \tag{5.2}$$

In the 'under-alloy' conditions, the contact resistance and the AlGaAs resistance become

$$R_C = R_{C1} \tag{5.3}$$

$$R_{Sch} = R_{Sch1} \tag{5.4}$$

Then, equation (5.2) assumes the form of

$$R_{access} \approx R_{C1} + R_{Cap} + R_{Sch1} + R_{CS} + R_{2DEG} \tag{5.5}$$

In the case of optimally alloyed contacts at 430°C, the resistances become

$$R_C = R_{C2} \tag{5.6}$$

$$R_{Sch} = R_{Sch2} \approx \frac{R_{Sch1}}{100} \tag{5.7}$$

This is illustrated in figure 5.22. The access resistance can then be evaluated as

$$R_{access} \cong R_{C2} + R_{Sch2} \approx R_{C2} + \frac{R_{Sch1}}{100} \tag{5.8}$$

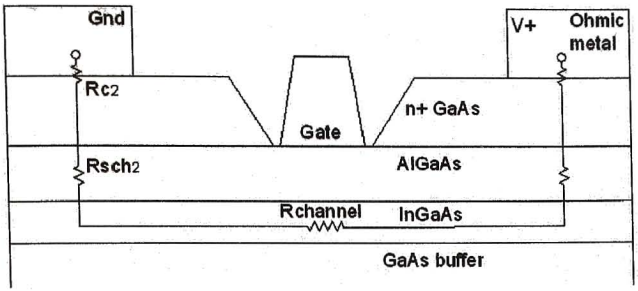



**Figure. 5.22. Current flow path for optimally alloyed pHEMTs indicating the components of access resistances.**

In this condition, the resistances of $R_{Cap}$, $R_{CS}$ and $R_{2DEG}$ can be assumed to be negligible. Thus, doping of the device layers, especially the AlGaAs layers, plays a dominant part.

### 5.2.4.2. Device parameters

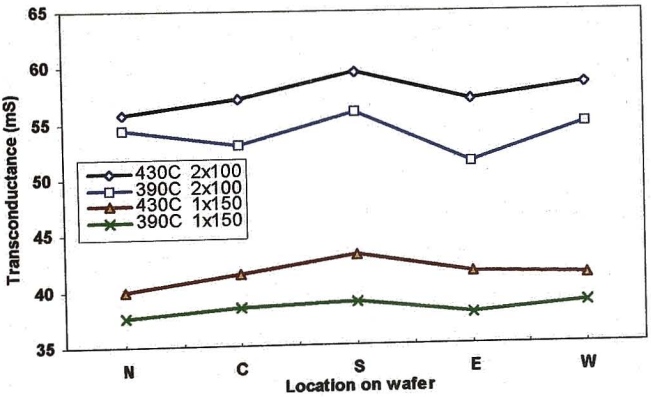



**Figure 5.23. $g_m$ values at $V_{gs}$ = 0V of 1 x 150μm and 2 x 100μm pHEMTs**

The transconductance ($g_m$) of 1 x 150μm and 2 x 100μm FETs, which have 0.5μm gate lengths and a source-drain spacing of 6μm, was measured on samples A and D. Figure 5.23 shows the $g_m$ values at $V_{gs}$ = 0V for both the above devices. The difference between the $g_m$ values shows evidence of improvement due to change of

alloying cycle. The above samples were RF characterized and the cut-off frequencies of the 2 x 100μm devices were between 36.0-39.0GHz.

### 5.3. Conclusion

Very low $R_c$ values were obtained for alloying at 430°C. During this work, we have shown that eventhough the channel is contacted at 390°C, alloying at 430°C was necessary for sufficiently doping the $n^+$ and the AlGaAs layers upto the channel, in order to achieve very low contact resistances. Doping levels of Ge in all the device layers below the contact pads seems to be the critical factor which controls or limits low contact resistances. It was established that the AlGaAs layers offered higher resistance and retard diffusion of alloy materials. Hence, the diffusion constant of germanium in pHEMTs was lower than that of MESFETs, leading to the requirement of higher alloy temperatures.

It has been proposed that the access region was vertically below the contact pads, through the 'reacted' semiconductor regions including the AlGaAs layers. Current flow in other regions may be negligible, even for the 'under-alloy' conditions.

The roughness of the contact surface was observed to follow the trend of contact resistance with temperature. The minimum surface roughness was observed for the optimum alloy condition.

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# Chapter VI

## Conclusions

### 6.1. Summary

In this thesis, ohmic contacts to MESFETs and pseudomorphic HEMTs were studied with a view to achieving low contact resistances and understanding its formation. Detailed structural and electrical characterizations of the contacts were carried out using techniques such as SIMS, TEM, thermal imaging, and the device performances. The contact surface morphology was characterized by AFM, TEM and SEM to understand the correlation to low resistance contact formation. Influence of implant activation in MESFETs on ohmic contacts was also studied.

During this work, techniques such as thermal imaging and AFM were adapted for characterizing ohmic contacts.

#### 6.1.1. Ohmic contacts to MESFETs

Low contact resistances of the order of 0.05-0.07Ω-mm were achieved after optimally alloying at 400°C for 150 sec. From the backside SIMS studies, indiffusion of the constituents of contact metallisation, viz., Au, Ge and Ni was observed. The concentration profile of Ge was found to extend about 1000Å into the channel layer. This established the sufficient condition that along with the $n^+$-contact layer, the $n^+$-n interface and the peak concentration region of the channel were to be degenerately doped for achievement of very low contact resistances.

While Ni formed compounds with Ge and As to assist the doping of Ge, the indiffusion of Au was found to be the critical requirement for Ge doping and formation of Ge-rich compounds. The Au and Ni concentration profiles followed the profile of Ge. A low diffusion constant of $2.1 \times 10^{-10}$ $cm^2$/sec was obtained from diffusion calculations.

The current flow into the channel takes the highly doped path below the contact pads, forming a longitudinal component of the access resistance. This extended definition of the access region was validated by thermal imaging and device performances.

A correlation of surface morphology with contact resistance was established. Very low RMS roughness was obtained for optimum alloying. The role of outdiffusion was understood to be the cause of deterioration of surface morphology with temperature.

The optimally alloyed contacts were found to be thermally stable and reliable. The cumulative effects of thermal treatments during device processing did not affect the electrical behaviour of the contacts. SIMS analysis showed that the amount of interdiffusion at the 'final' processing stage was minimal. Accelerated life tests did not introduce serious drifts in contact resistance. Very low drifts of +13% in the 'final' contact resistances were observed.

### 6.1.2. Influence of activation on ohmic contacts

Activation annealing experiments resulted in achieving low sheet resistivities of 160Ω/□ for the optimum anneal cycle of 955°C for 25 sec. Maximum activation of about 60% and 85% were simultaneously obtained for the $n^+$ and channel implants, respectively, for this anneal cycle. It was also observed that the 'tail' region of the channel implant was shallow and peak concentration region was higher. This was validated by lower pinch-off voltages and high transconductances.

The ohmic contact resistance was observed to decrease with annealing temperature and was lowest for optimum annealing at 955°C with values of 0.06 Ω-mm. Increase in the concentration of the peak region of the channel favoured the reduction of the resistance of the $n^+$-n interface. This minimized the possibility of Joule heating at this interface. When wafers with high activation were optimally alloyed, the $n^+$-n interface gets degenerately doped enabling direct current flow into channel. Contact resistance was thus dependent on the reduction in the resistance of the $n^+$-n interface region.

### 6.1.3. Ohmic contacts to pseudomorphic HEMTs

Alloying experiments on pHEMT wafers were carried out to obtain low contact resistances of 0.05-0.07 Ω-mm. Eventhough the channel was contacted at 390°C, alloying at 430°C was critical and necessary for sufficiently doping the $n^+$ and AlGaAs layers upto the channel, and thereby leading to low contact resistances.

Backside SIMS investigations have shown that the diffusion constant of 1.71 x $10^{-11}cm^2/sec$ of germanium in pHEMTs was lower than that of the MESFET device layers, leading to the requirement of higher alloy temperatures. It was established that the AlGaAs layers offered higher resistance and retard diffusion of alloy materials.

It was proposed that the access region for conduction of source-drain current was vertically below the contact pads, through the 'reacted' semiconductor regions including the AlGaAs layers, even for the 'under-alloy' conditions.

The roughness of the contact surface was observed to follow the trend of contact resistance with temperature. The minimum surface roughness was observed for the optimum alloy condition.

## 6.2. Scope for future work

During this thesis work, while studying the ohmic contact formation in MESFETs and pHEMTs, some aspects pertaining to further improvements in contact formation methods were identified as scope for future work. Development of low resistance ohmic contacts to metamorphic HEMTs and GaN-based devices will extend the functional domain of MMICs. They are briefly described below:

### 6.2.1. Use of diffusion barrier

It was found that outdiffusion increases with alloying temperature. This deteriorates the surface morphology as well as creates stoichiometric imbalance in the $n^+$ surface layers. This can only be preserved by incorporating a diffusion barrier such as Ag, Ti, Pt, etc [1] between the AuGe/Ni layer and the Au overlayer. This layer prevents the intermixing of the overlayer Au with the eutectic, which increases Ga outdiffusion from the surface. This also increases the process window and reduces the sensitivity to alloying temperatures. In pseudomorphic HEMT devices, issues like surface morphology play a dominant role in limiting the contact resistances. Investigations of this approach can lead to lower contact resistances with better surface morphology.

### 6.2.2. Selective implantation

Formation of direct ohmic contacts into the channel of MESFETs was found to improve device performances. This could be enhanced by selective implantation

methods, where high-doped regions or 'trenches' facilitating a direct current flow path to the channel could be formed. This can enormously improve the performance of MESFETs.

### 6.2.3. Low resistance contacts to metamorphic HEMTs

Metamorphic HEMTs (M-HEMTs) are important high frequency device structures. The ohmic contact process to M-HEMTs requires a stringent choice of alloy parameters. Eventhough an $n^+$ InGaAs layer is used for easy fabrication of ohmic contacts, the low resistance contact formation mechanisms are not well understood. Investigations into these aspects will greatly benefit the future requirements in MMICs.

### 6.2.4. Ohmic contacts to GaN-based devices

The most widely used contact material to n-type GaN is based on Al/Ti. It is reported that the Ti layer forms a degenerate layer or reduces surface oxides [2]. The other means to heavily dope the surface has been by diffusion or ion implantation of Si or by epitaxially growing $n^+$-InGaN layers. Development of suitable ohmic contacts to GaN-based microwave devices will be beneficial for the next generation MMICs. Obtaining low contact resistances to p-type GaN devices has been difficult due to large acceptor ionization energy and difficulty in achieving high free hole concentrations. This new area of research will greatly benefit low threshold laser fabrication.

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1. Transmission electron microscopy characterization of electronic materials and device structures, D. V. Sridhara Rao, **G. Sai Saravanan**, K. Muraleedharan, R. Balamuralikrishnan, R. Muralidharan and H. P. Vyas, *Metals, Materials and Processes, 2007, Vol. 19, No 1-2 (in press).*
2. Direct ohmic contacts to rapid thermal alloyed pseudomorphic HEMTs with low contact resistance due to improved alloy penetration through AlGaAs layers, **G.Sai Saravanan**, Mahadeva Bhat. K, K. Muraleedharan, H. P. Vyas, R. Muralidharan and A. P. Pathak, *communicated to Semiconductor Science and technology, 2007.*
3. Influence of activation of $Si^{29+}$ ion-implantation in GaAs on ohmic contact resistance and electrical performances of MESFETs, **G. Sai Saravanan**, Mahadeva Bhat. K, H. P. Vyas, K. Muraleedharan and A. P. Pathak, *Under review, Radiation effects and defects in solids, 2007.*
4. Outdiffusion-influenced morphological evolution of rapid thermal alloyed AuGe/Ni/Au ohmic contacts to MESFETs, **G. Sai Saravanan**, Mahadeva Bhat. K, S. Dhamodaran, D. V. Sridhara Rao, K. Muraleedharan, R. Balamuralikrishnan, R. Muralidharan, H. P. Vyas, and A. P. Pathak, *communicated to Thin Solid Films, 2007.*
5. Low resistance ohmic contact formation due to enhanced diffusion of germanium and correlation to electrical performance of MESFETs and MMICs, **G. Sai Saravanan**, Mahadeva Bhat. K, Sandeep Chaturvedi, H. P. Vyas, K. Muraleedharan and A. P. Pathak, *communicated to J. Microelectronic Engineering, 2007.*
6. *Low- and high-energy irradiations of InGaAs /GaAs heterostructures: a comparison, S. Dhamodaran, A. P. Pathak, D. K. Awasti, R. Muralidharan, **G. Sai Saravanan**, B. Sundaravel, R. Kesavamurthy and K. G. M. Nair, *Radiation effects and defects in solids, 2007 (in press).*

## *To be communicated*

1. Accelerated thermal aging and backside SIMS analysis of optimally alloyed ohmic contacts to MESFETs with low drifts, **G. Sai Saravanan**, Mahadeva Bhat K, H. P. Vyas, R. Muralidharan, K. Muraleedharan and A.P. Pathak.

## *Conferences/Workshop*

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4. Manufacturing at GAETEC: Influence of ohmic contacts on power output of X-band medium power MMICs, Invited talk in *Symposium on GaAs devices and MMICs at Solid State Physics Laboratory, Delhi, 22nd Feb '05.*

(* Not included in present thesis)

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